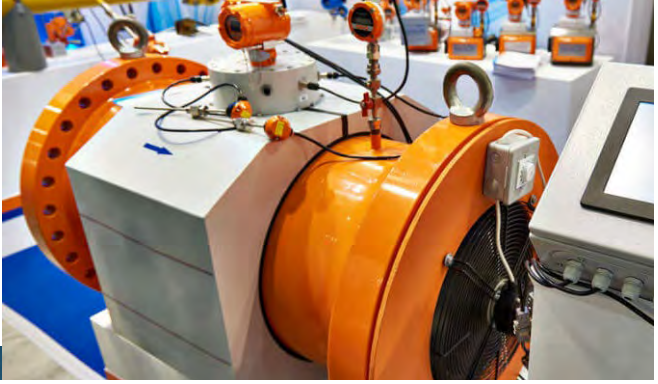
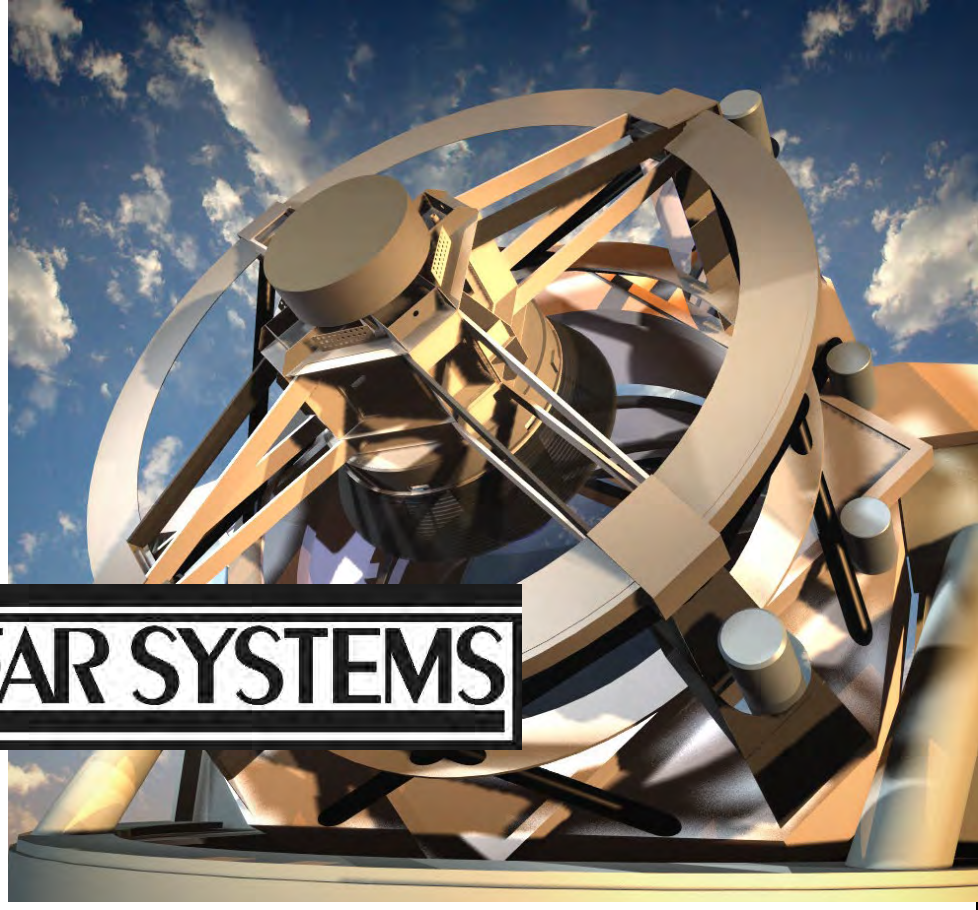




LINEAR SYSTEMS

Linear Systems

2022 DATA BOOK

Quality Through Innovation Since 1987

Table of Contents:

Table of Contents Continued:

Linear Systems'
2022 Data Book

Testimonials

"One of the main reasons we offer a lifetime warranty for our products is because we can count on Linear Systems. The Linear Systems' LSK389B J-FET is so reliable that in the rare event a faulty unit is discovered, it's the very last variable we check. The LSK389B J-FET simply doesn't fail!"

Rodger Cloud
www.cloudmicrophones.com

"I believe that selecting Linear Systems' LSJ74 for our Halo Integrated Amplifier has contributed to the unprecedented number or rave reviews and awards it's received. Parasound's product development team commends Linear Systems for providing customer support that is top-notch."

Richard Schram
www.parasound.com

"Our QCL instrument has the lowest noise commercially available and is used for pharmaceutical process quality control and trace gas emissions monitoring. Noise testing the instrument is critical to ensuring performance. Our test equipment uses the Linear Systems' LSK389 JFET. The precision of the LSK389 makes verifying the precision of our instruments possible."

Lisa Mueller
www.teamwavelength.com

Introduction

Welcome to the 2022 edition of the Linear Systems Data Book. Here we present all our devices in one single document to give you a complete overview of our portfolio. We hope that makes it even easier for you to find the right product for your design. Our extensive portfolio offers high-quality discrete components serving a wide range of markets including automated test equipment, professional audio, medical electronics, military and test & measurement. Our products are housed in some of the most advanced, industry-leading small packages, as well as robust industry standard packages giving designers many options. Alongside quality and efficiency, Linear Systems' customers value reliability and a constant supply they can trust. We produce consistently reliable discrete components and we work at every step to safeguard the long-term availability of our manufacturing processes and products, to ensure secure supply for all our customers. In addition, Linear Systems has an on-site testing facility to conduct a full range of production and post-production testing. Specialized capabilities include: Hi-temperature product testing and the highest capacity sub-nanovolt noise production testing capability in the world. We have a long history in the business and broad range of experience. Linear Systems ensures dedicated in-house technical support – from simplifying selection via quick-reference material to in-person technical meetings with our engineering team. All to help you choose the best devices for the most efficient design.

This Data Book provides all Linear Systems' datasheets in one spot. The Table of Contents includes product category, part number and part description, so you can browse the entire product line with ease. There is also a dedicated section on packages, highlighting the latest package innovations and packing options.

Linear Systems has been manufacturing high-quality discrete components for over 30 years. We offer improved and direct replacements for over 2,000 current and discontinued small signal discretes from Fairchild, Vishay-Siliconix, Analog Devices, Interfet, Intersil, Motorola, ON Semiconductor, Toshiba, NXP and National Semiconductor. Whether you have a new or existing design, Linear Systems can provide the discrete component(s) to best fit your application.

Ordering Information and Sampling Policy

Linear Systems does not impose minimum order requirements when ordering directly from the factory. We understand customers may only need a few parts for prototyping, repairs, student projects or DIY designs. Our parts are available to all. We do, however, offer incremental price breaks for increased purchase quantity. Linear Systems also supports customers who require very large quantities for mass production. In this case special high-quantity pricing may be negotiated for bulk purchases of 100,000 plus pieces.

Do you use the LTspice® electronic circuit simulator? The majority of Linear Systems' parts are included in the latest edition of the LTspice® embedded library. Customers often try our products through the LTspice-simulator before ordering.

Would you like to receive samples? Samples including detailed data logs are available upon request.

Interested in a part not listed on our website, or do you need a custom part? Linear Systems offers many non-standard electrical screening and package options.

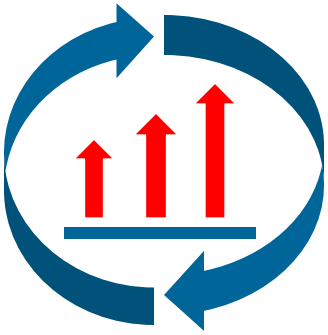
Linear Systems' friendly staff are here to help. For any kind of assistance you can reach us by calling (510) 490-9160 or email us at support@linearsystems.com.

Our Commitment:

Quality and Reliability

Quality is Everything

Linear Systems is ISO 9001:2015 certified. All our processes and manufacturing facilities are subject to regular internal audits.



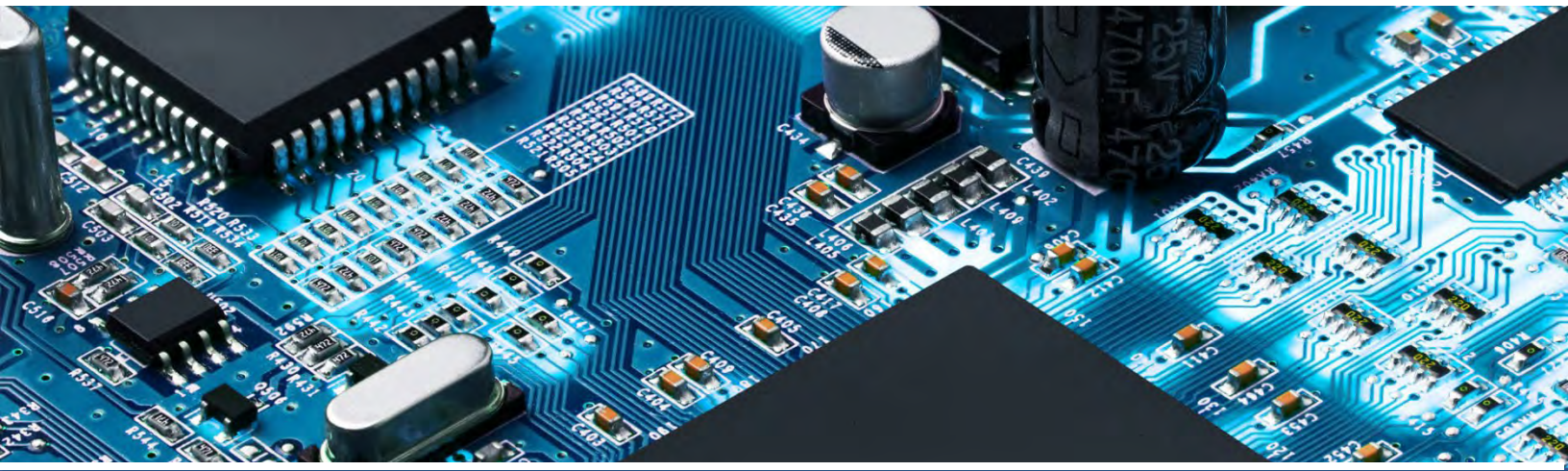
Continuously Improve

Linear Systems' Continuous Improvement Program (CIP) ensures that existing processes are strategically reviewed while each new development builds on past learning. The result is that best practices are always employed.

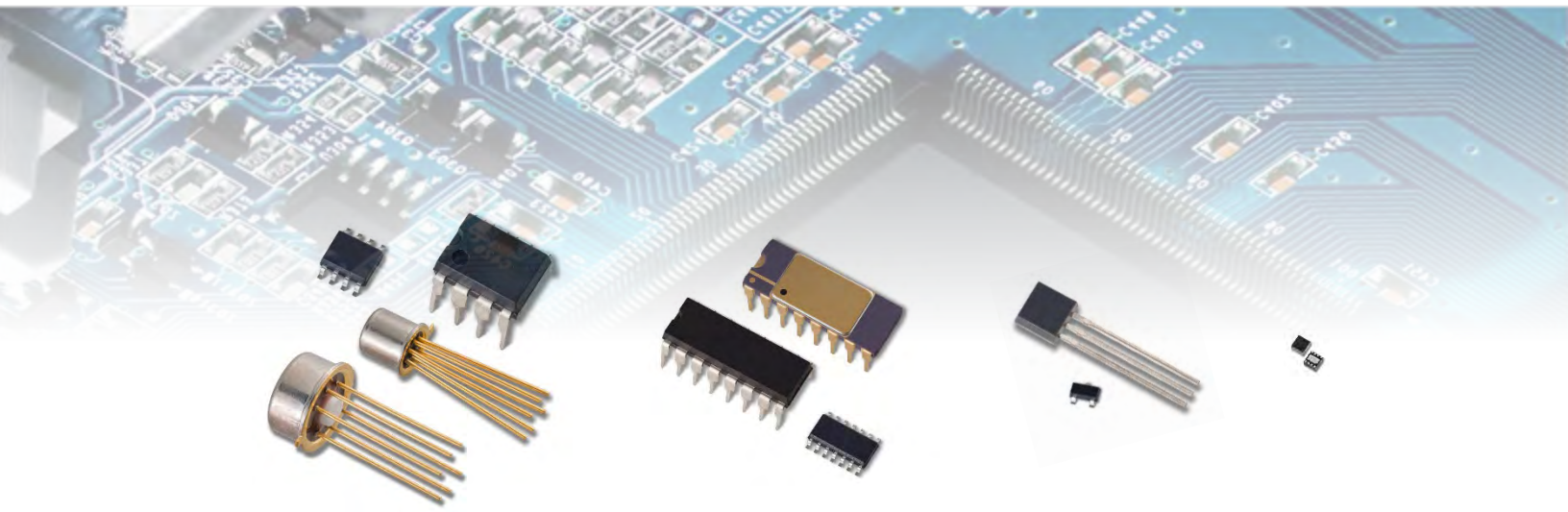
Zero Defect

Zero defect is our goal. To ensure continuous improvement, failure analysis and the determination to find root causes is performed at all stages of development and production by adoption of quality-analysis tools and methods.

LINEAR SYSTEMS Quality Through Innovation Since 1987



DISCRETE COMPONENT PRODUCT LINE

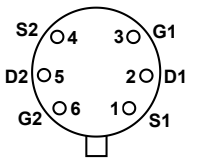


LSK389 A/B/C/D

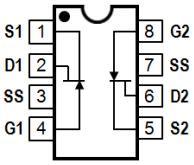
Ultra-Low Noise Monolithic Dual N-Channel JFET Amplifier

INDUSTRY'S FIRST 100% TESTED LOWEST NOISE JFET

Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation @ +25°C	400mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = 40V
Gate to Drain	V_{GDS} = 40V



TO-71 6L
Top View



SOIC 8L
Top View

Features

- Ultra-Low Noise: e_n = 1.3nV/√Hz (typ), f = 1.0kHz and NBW = 1.0Hz
- Ultra-Low Noise: 1.5nV/√Hz (typ), f = 10Hz and NBW = 1.0Hz
- Tight Matching: $|V_{GS1-2}|$ = 15mV max
- High Breakdown Voltage: BV_{GSS} = 40V max
- High Gain: G_{fs} = 20mS (typ)
- Low Capacitance: 25pF (typ)
- Improved Second Source Replacement for 2SK389

Benefits

- Improved System Noise Performance
- Unique Monolithic Dual Design Construction of Interleaving Both JFETs on the Same Piece of Silicon
- Excellent Matching and Thermal Tracking
- Great for Maximizing Battery Operated Applications by Providing a Wide Output Swing
- A High Signal to Noise Ratio as a Result of the LSK389's Low and Tightly Matched Gate Threshold Voltages

Applications

- Audio Amplifiers and Preamps
- Discrete Low-Noise Operational Amplifiers
- Battery-Operated Audio Preamps
- Audio Mixer Consoles
- Acoustic Sensors
- Sonic Imaging
- Instrumentation Amplifiers
- Microphones
- Sonobouys
- Hydrophones
- Chemical and Radiation Detectors

Description

The LSK389 is the industry's lowest noise Dual N-Channel JFET, 100% tested, guaranteed to meet 1/*f* and broadband noise specifications, while eliminating burst (RTN or popcorn) noise entirely. The LSK389 Series, Monolithic Dual N-Channel JFETs were specifically designed to provide users a better performing, less time consuming and cheaper solution for obtaining tighter IDSS matching, and better thermal tracking, than matching individual JFETs. The LSK389's features incorporate four grades of IDSS: 2.6-6.5mA, 6.0-12.0mA, 10.0-20.0mA and 17-30mA, with an IDSS match of 10 percent, a gate threshold offset of 15mV, a voltage noise (en) of 1.3nV/√Hz typical at f = 1.0kHZ, with a Gain of 20mS typical, and 25pF of capacitance typical. The LSK389 provides a wide output swing, and a high signal to noise ratio as a result of the LSK389's tightly matched and low gate threshold voltages. The 40V breakdown provides maximum linear headroom in high transient program content amplifiers.

Additionally, the LSK389 provides a low input noise to capacitance product that has nearly zero popcorn noise. The narrow ranges of the IDSS electrical grades combined with the superior matching performance of the LSK389's monolithic dual construction promote ease of device tolerance in low voltage applications, as compared to matching single JFETs. Available in surface mount SOIC 8L and thru-hole TO-71 6L packages.

Contact the factory for tighter noise and other specification selections. For equivalent single N-Channel version, please refer to the LSK170 datasheet.

Electrical Characteristics @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage		-40	---	---	V	V_{DS} = 0, I_D = -100µA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage		-0.3	---	-1.6	V	V_{DS} = 10V, I_D = 0.1µA
I_{DSS}	Drain to Source Saturation Current	LSK389A	2.6	---	6.5	mA	V_{DS} = 10V, V_{GS} = 0
		LSK389B	6	---	12		
		LSK389C	10	---	20		
		LSK389D	17	---	30		
I_{GSS}	Gate to Source Leakage Current		---	-100	-300	pA	V_{GS} = -25V, V_{DS} = 0
I_{G1G2}	Gate to Gate Isolation Current		---	±1.0	±50	nA	V_{G1-G2} = ±45V, I_D = I_S = 0A
G_{fs}	Full Conduction Transconductance		8	20	---	mS	V_{DS} = 10V, V_{GS} = 0, *f* = 1kHz
e_n	Noise Voltage		---	1.3	1.9	nV/√Hz	V_{DS} = 10V, I_D = 2mA, *f* = 1kHz, NBW = 1Hz
e_n	Noise Voltage		---	1.5	4.0	nV/√Hz	V_{DS} = 10V, I_D = 2mA, *f* = 10Hz, NBW = 1Hz
C_{ISS}	Common Source Input Capacitance		---	25	---	pF	V_{DS} = 10V, V_{GS} = 0, *f* = 1MHz,
C_{RSS}	Common Source Reverse Transfer Cap.		---	5.5	---	pF	V_{DG} = 10V, I_D = 0, *f* = 1MHz,

Matching Characteristics @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate to Source Cutoff Voltage	---	6.0	15	mV	V_{DS} = 10V, I_D = 1mA
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.9	1.0	1.1	n/a	V_{DS} = 10V, V_{GS} = 0V

Notes

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

Typical Characteristics

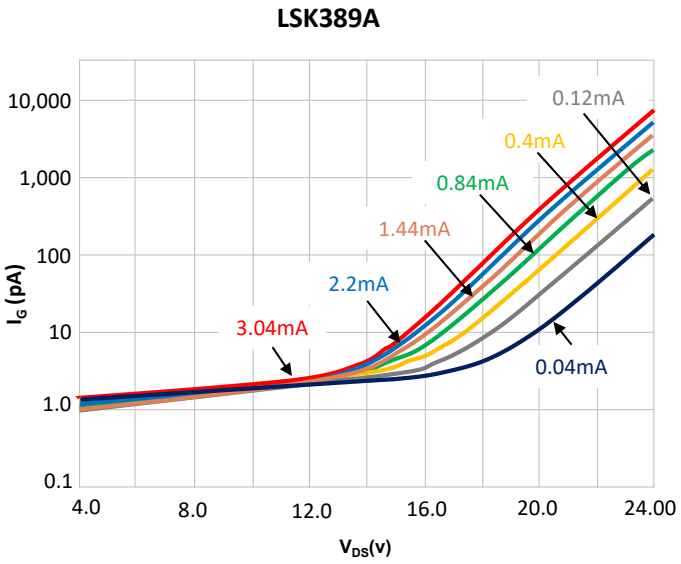


Figure 1. Gate Current (I_G) vs. V_{DS} vs. I_D

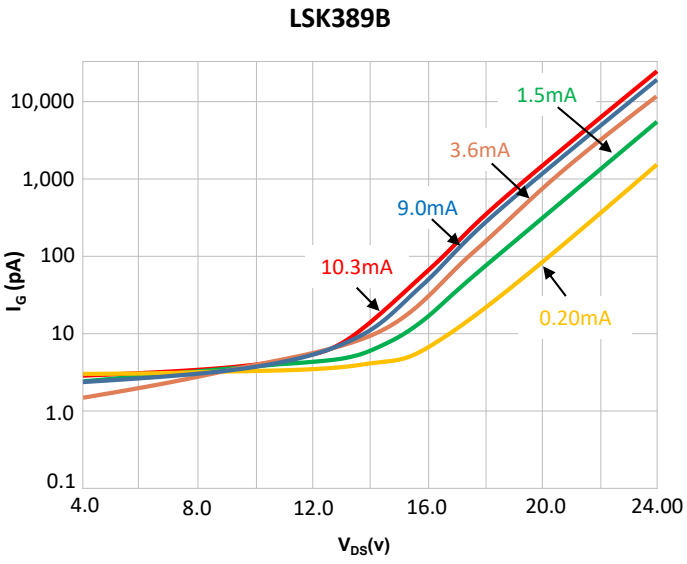


Figure 2. Gate Current (I_G) vs. V_{DS} vs. I_D

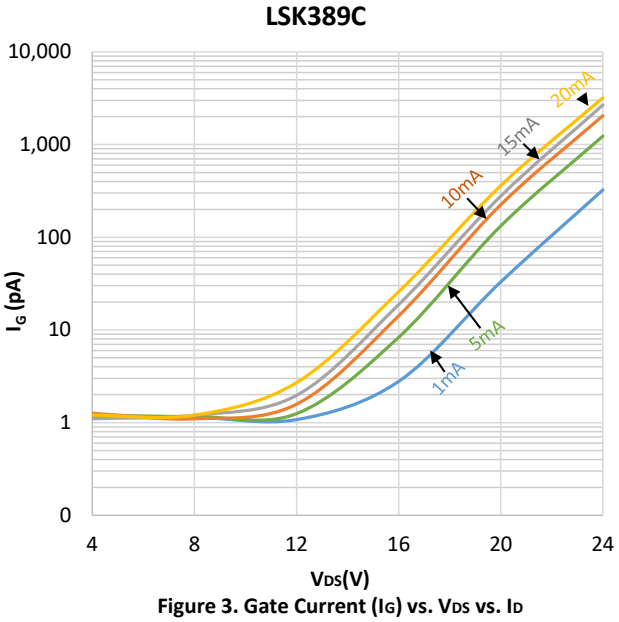


Figure 3. Gate Current (I_G) vs. V_{DS} vs. I_D

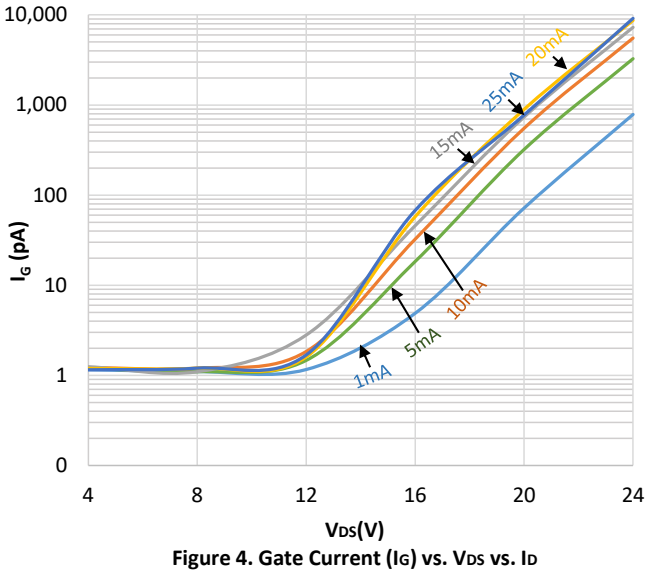


Figure 4. Gate Current (I_G) vs. V_{DS} vs. I_D

Typical Characteristics Continued

LSK389A

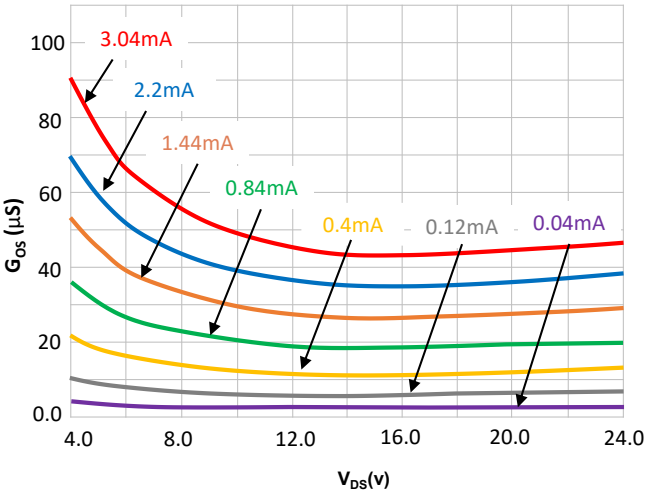


Figure 5. Output Conductance - G_{OS} vs. V_{DS} vs. I_D

LSK389B

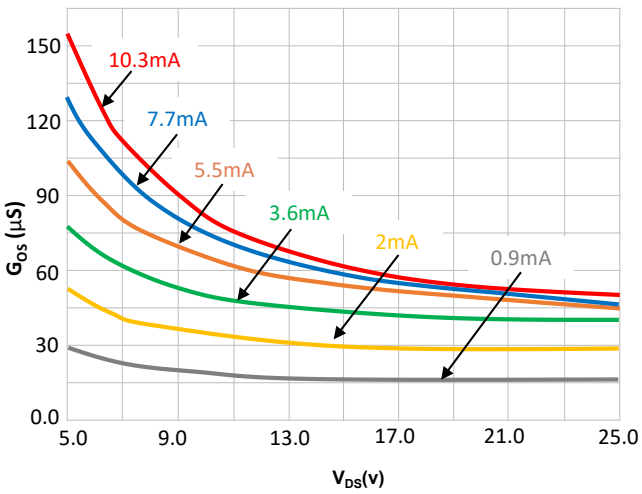


Figure 6. Output Conductance - G_{OS} vs. V_{DS} vs. I_D

LSK389C

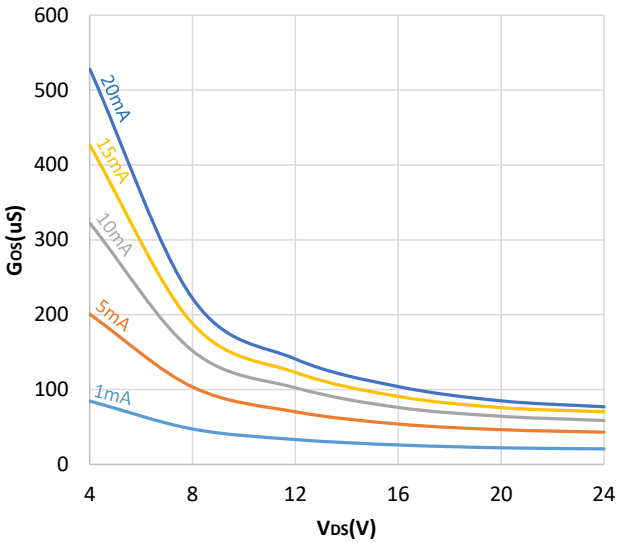


Figure 7. Output Conductance - Gos vs. VDS vs. ID

LSK389D

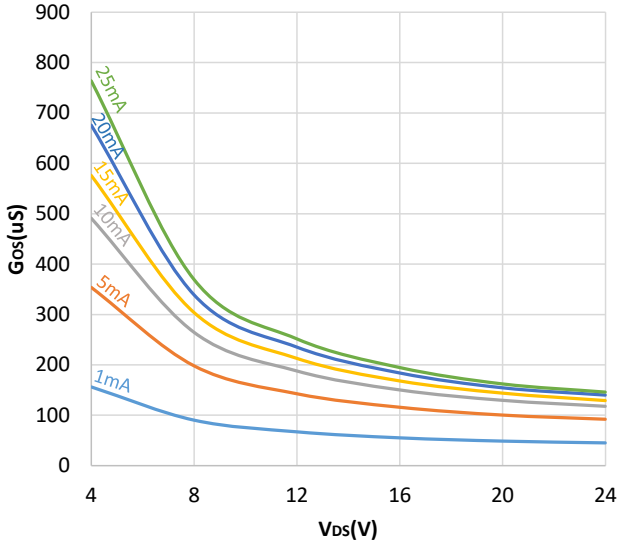


Figure 8. Output Conductance - Gos vs. VDS vs. ID

Typical Characteristics Continued

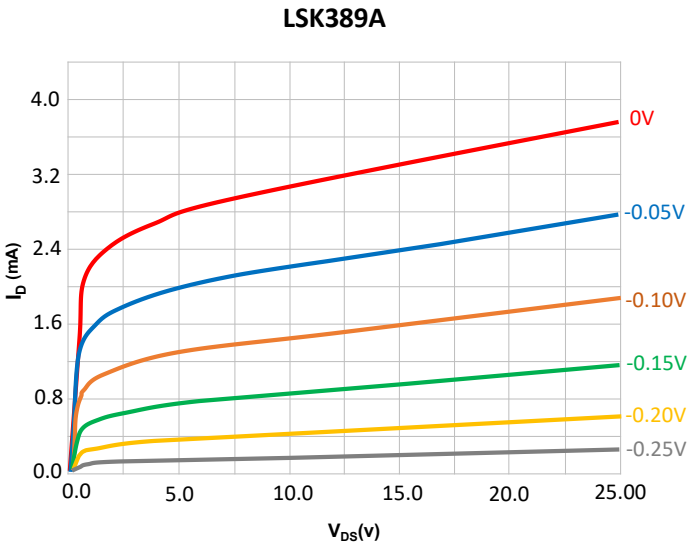


Figure 9. I_D vs. V_{DS} vs. V_{GS}

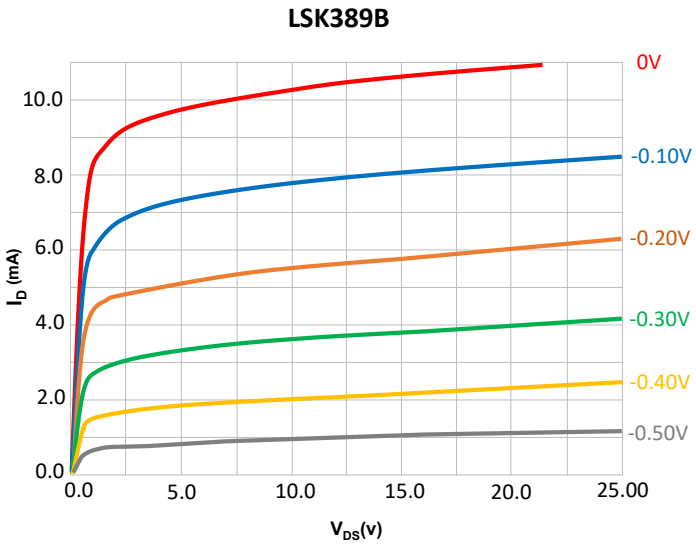


Figure 10. I_D vs. V_{DS} vs. V_{GS}

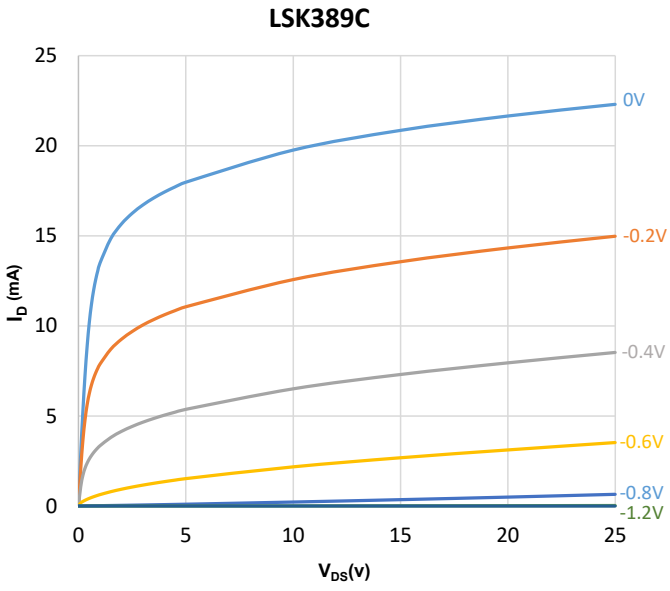


Figure 11. I_D vs. V_{DS} vs. V_{GS}

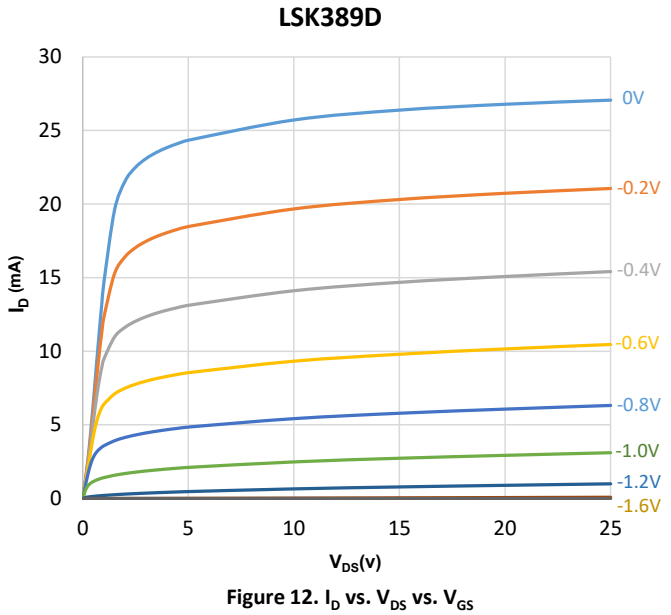


Figure 12. I_D vs. V_{DS} vs. V_{GS}

Typical Characteristics Continued

LSK389A

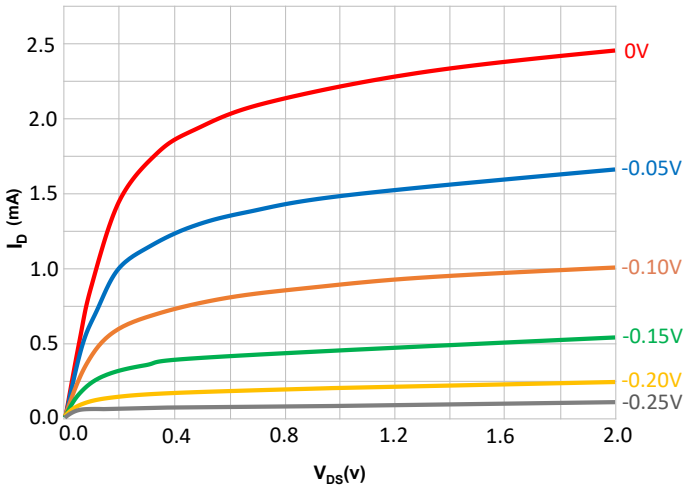


Figure 13. I_D vs. V_{DS} vs. V_{GS}

LSK389B

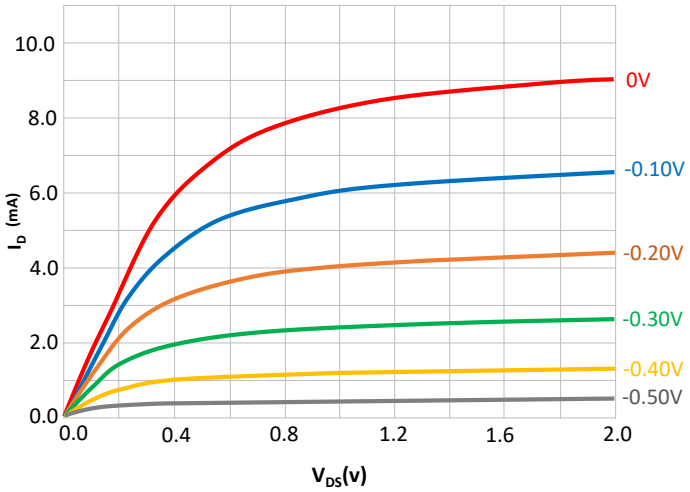


Figure 14. I_D vs. V_{DS} vs. V_{GS}

LSK389C

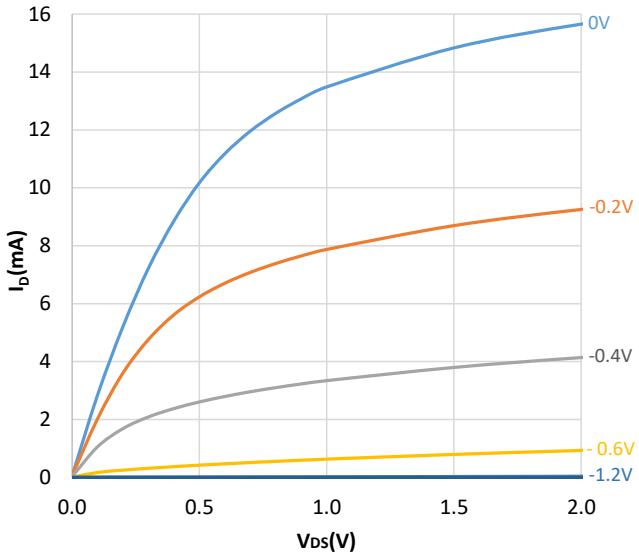


Figure 15. ID vs. VDS vs. VGS

LSK389D

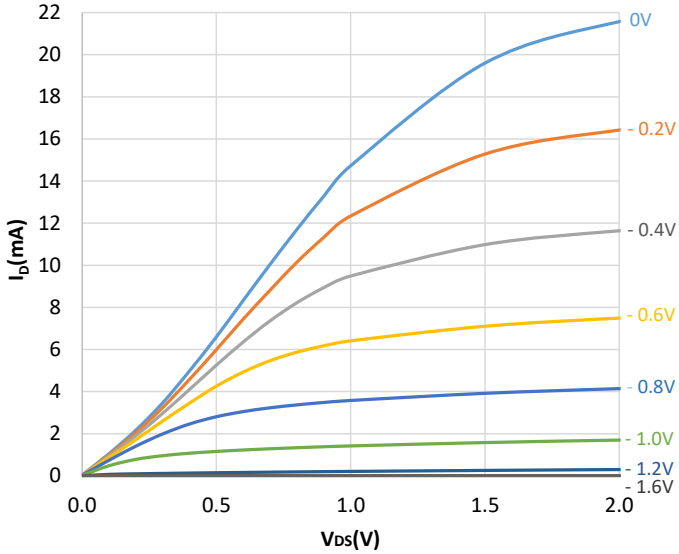


Figure 16. ID vs. VDS vs. VGS

Typical Characteristics Continued

Common Source Forward Transconductance vs. Drain Current
LSK389A & B

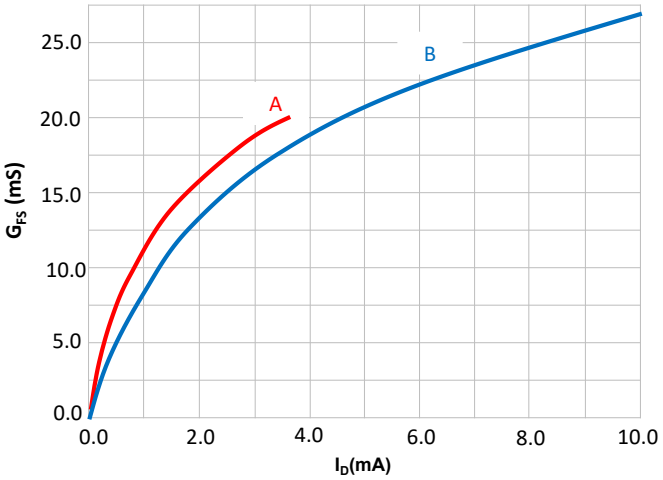


Figure 17. G_{FS} vs. I_D

Common Source Forward Transconductance vs. Drain Current
LSK389C & D

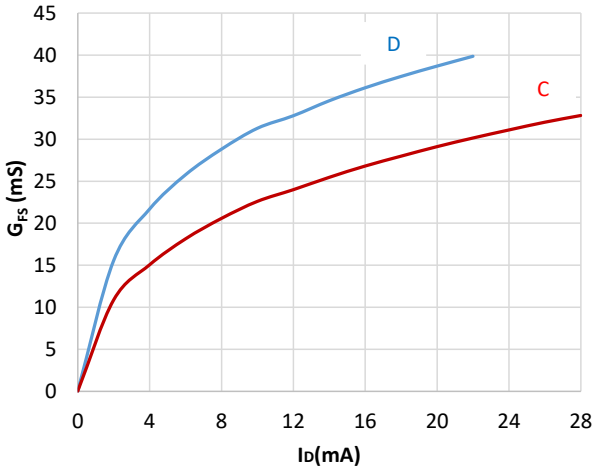


Figure 18. G_{FS} vs. I_D

LSK389A & B

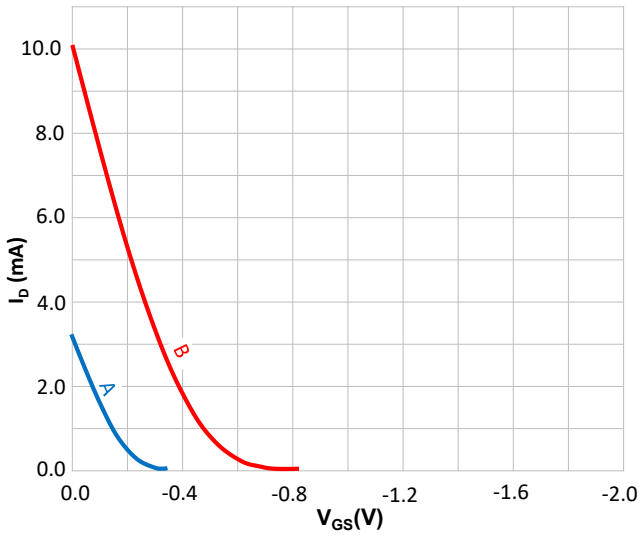


Figure 19. I_D vs. V_{GS}

LSK389C & D

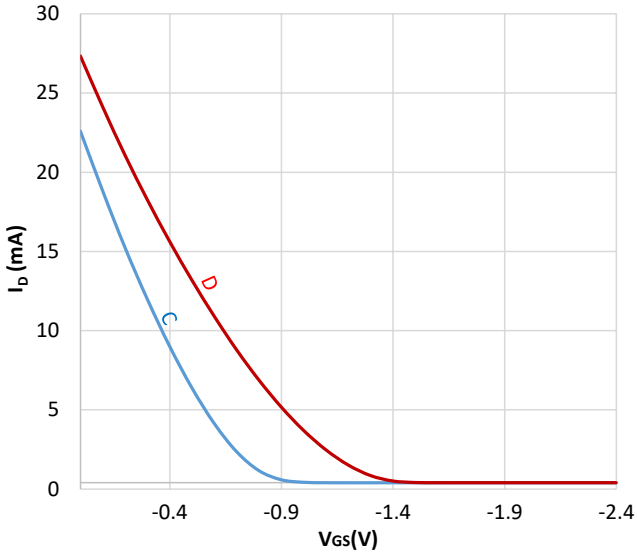


Figure 20. I_D vs. V_{GS}

Typical Characteristics

Drain Current Transconductance vs. Gate-Source Cutoff Voltage

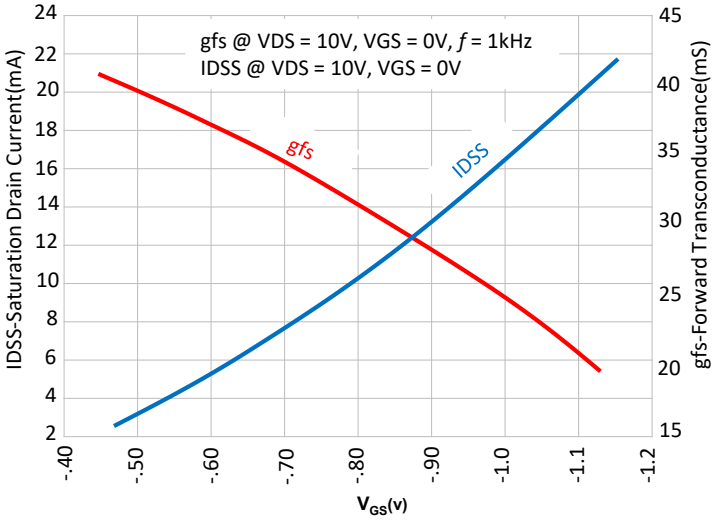


Figure 21. V_{GS} (cutoff) vs. I_{Dss} vs. G_{FS}

Equivalent Input Noise Voltage vs. Frequency

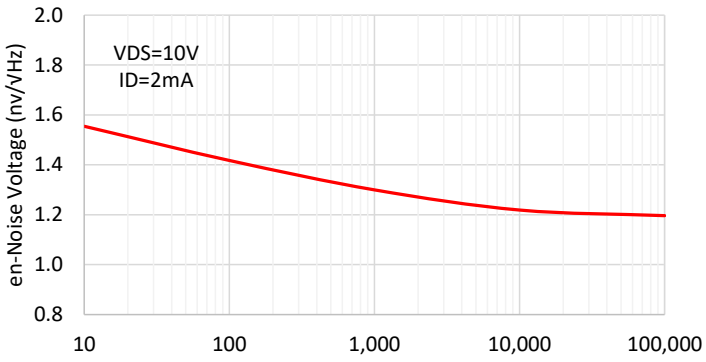
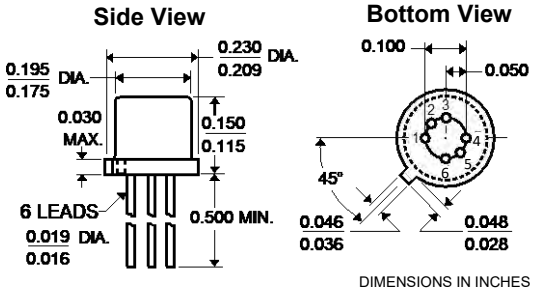


Figure 22.
f - Frequency (Hz)

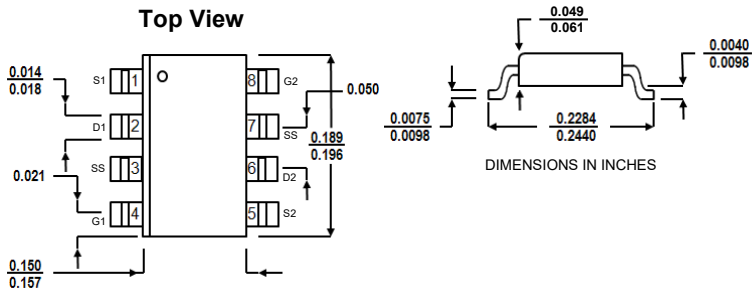
Package Dimensions

TO-71 6 Lead



DIMENSIONS IN INCHES

SOIC 8 Lead



DIMENSIONS IN INCHES

SS: SUBSTRATE, LEAVE THESE PINS FLOATING (N/C)

Ordering Information

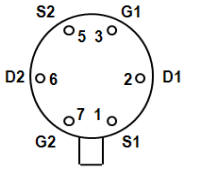
Standard Part Call-Out
LSK389A/B/C or D TO-71 6L RoHS
LSK389A/B/C or D SOIC 8L RoHS
Custom Part Call-Out (Custom Parts Include SEL + 4 Digit Numeric Code)
LSK389A/B/C or D TO-71 6L RoHS SELXXXX
LSK389A/B/C or D SOIC 8L RoHS SELXXXX

LSK489

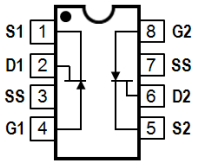
Low Noise, Monolithic Dual N-Channel JFET Amplifier

INDUSTRY'S LOWEST INPUT CAPACITANCE MONOLITHIC DUAL N-CHANNEL JFET

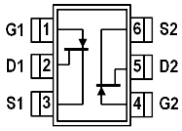
Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation, TA = 25°C	
Continuous Power Dissipation, per side [4]	300mW
Power Dissipation, total [5]	500mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = 60V
Gate to Drain	V_{GDS} = 60V
Features	
Ultra Low Noise	e_n = 1.8nV/√Hz
Low Input Capacitance	Ciss = 4pF



TO-71
Top View



SOIC-A
Top View



SOT-23
Top View

* For equivalent single version, see LSK189

Features

- Low Noise: e_n = 2nV/√Hz (typ), *f* = 1kHz, NBW = 1Hz
- Very Low Common Source Input Capacitance of C_{ISS} = 4pF – typ and 8pF- max
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage I_{GSS} and I_G
- High CMRR 102 dB

Benefits

- Tight Differential Voltage Match vs. Current
- Improved Op Amp Speed Settling Time Accuracy
- Minimum Input Error Trimming Error Voltage
- Lower Intermodulation Distortion

Applications

- Wideband Differential Amplifiers
- High Speed Temperature Compensated Single Ended Input Amplifier Amps
- High Speed Comparators
- Impedance Converters
- Sonobouys and Hydrophones
- Acoustic Sensors

Description

The LSK489 is the industry's lowest input capacitance and low-noise monolithic dual N-Channel JFET. Low input capacitance substantially reduces intermodulation distortion. In addition, these dual JFETs feature tight offset voltage and low drift over temperature range, and are targeted for use in a wide range of precision instrumentation and sensor applications. The LSK489 is available in surface mount plastic SOIC 8L and SOT-23 6L, as well as thru-hole metal TO-71 6L packages. For an equivalent single N-Channel version refer to the LSK189 datasheet. LSK489 TO-71 6L and SOIC 8L are fit, form and pin compatible to the same LSK389 product.

The LSK489 provides a dramatic increase in capabilities for a wide range of low-noise applications.

The most significant aspect of the LSK489 is how it combines a noise level nearly as low as the LSK389 while having much lower gate-to-drain capacitance, 4pF versus the 25pF. The slightly higher noise of the LSK489, versus the LSK389, is not significant in most instances, while the much lower capacitance enables designers to produce simpler, more elegant circuit designs with fewer devices that cost less in production.

Like the Linear Systems LSK389, the LSK489 features a unique design construction of interleaving both JFETs on the same piece of silicon to provide excellent matching and thermal tracking, as well a low-noise profile having nearly zero popcorn noise.

LSK489

Matching Characteristics @ 25°C (unless otherwise stated)

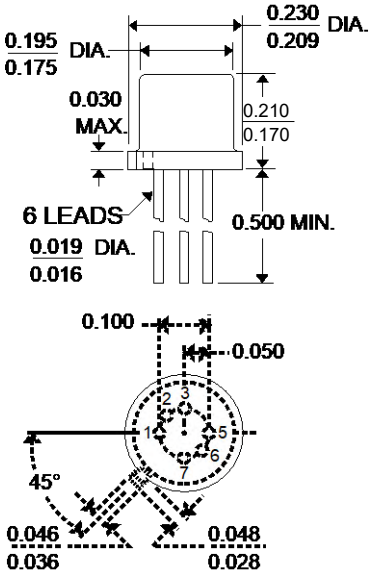
Symbol	Characteristic	Min.	Typ.	Max	Units	Conditions
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate to Source Cutoff Voltage			20	mV	V_{DS} = 10V, I_D = 1mA
$\frac{I_{DSS1}}{I_{DSS2}}$	Gate to Source Saturation Current Ratio	0.9		1.0		V_{DS} = 10V, V_{GS} = 0V
CMRR	**Common Mode Rejection Ratio** $-20 \log \lvert \Delta V_{GS1-2}/\Delta V_{DS} \rvert$	95	102		dB	V_{DS} = 10V to 20V, I_D = 200µA
e_n	Noise Voltage		2.0		nV/√Hz	V_{DS} = 15V, I_D = 2.0mA, *f* = 1kHz, NBW = 1Hz
e_n	Noise Voltage		3.5		nV/√Hz	V_{DS} = 15V, I_D = 2.0mA, *f* = 10Hz, NBW = 1Hz
C_{ISS}	Common Source Input Capacitance		4	8	pF	V_{DS} = 15V, I_D = 500µA, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Capacitance			3	pF	

Electrical Characteristics @ 25°C (unless otherwise stated)

Symbol	Characteristic	Min.	Typ.	Max	Units	Conditions
BV_{GSS}	Gate to Source Breakdown Voltage	-60			V	V_{DS} = 0, I_D = -1nA
$V_{(BR)G1 - G2}$	Gate to Gate Breakdown Voltage	±30	±45		V	I_G= ±1µA, I_D=I_S=0 A (Open Circuit)
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-1.5		-3.5	V	V_{DS} = 15V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage	-0.5		-3.5	V	V_{DS} = 15V, I_D = 500µA
I_{DSS}[2]	Drain to Source Saturation Current	2.5	5	15	mA	V_{DG} = 15V, V_{GS} = 0
I_G	Gate Operating Current		-2	-25	pA	V_{DG} = 15V, I_D = 200µA
			-0.8	-10	nA	T_A = 125°C
I_{GSS}	Gate to Source Leakage Current			-100	pA	V_{DG} = -15V, V_{DS} = 0
G_{fs}	Full Conductance Transconductance	1500			µS	V_{DG} = 15V, V_{GS} = 0, *f* = 1kHz
G_{fs}	Transconductance	1000	1500		µS	V_{DG} = 15V, I_D = 500µA
G_{OS}	Full Output Conductance			40	µS	V_{DG} = 15V, V_{GS} = 0
G_{OS}	Output Conductance		1.8	2.7	µS	V_{DG} = 15V, I_D = 200µA
NF	Noise Figure			0.5	dB	V_{DS} = 15V, V_{GS} = 0, R_G = 10MΩ, *f* = 100Hz, NBW = 6Hz

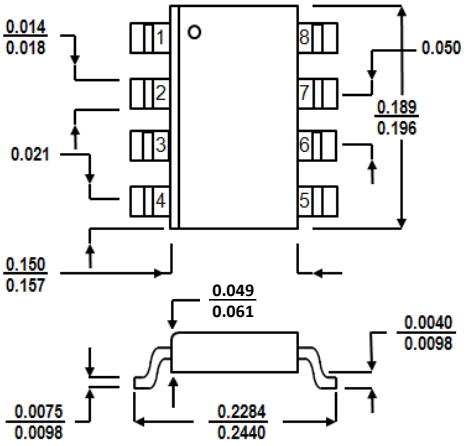
Package Dimensions

TO-71
Six Lead



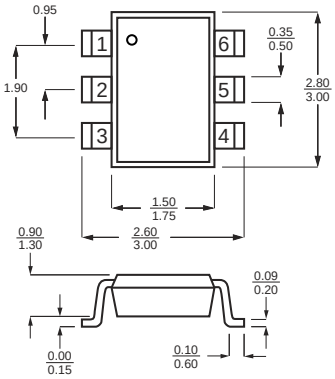
DIMENSIONS IN INCHES

SOIC-A
8 Lead



DIMENSIONS IN INCHES

SOT-23
Six Lead

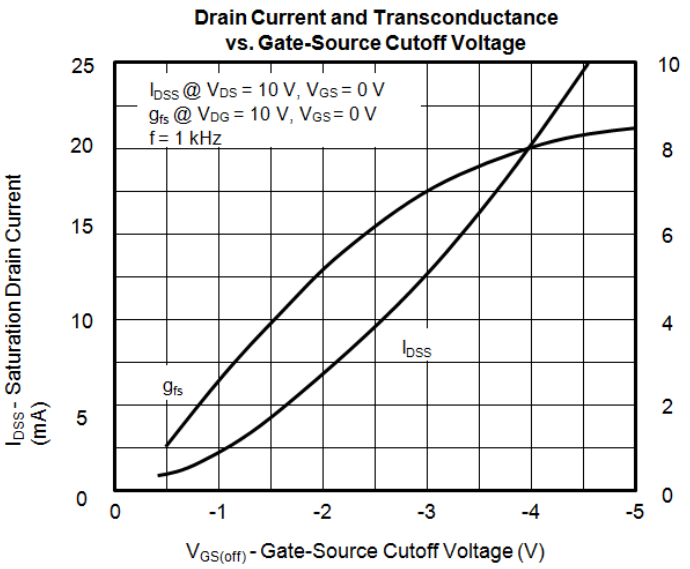


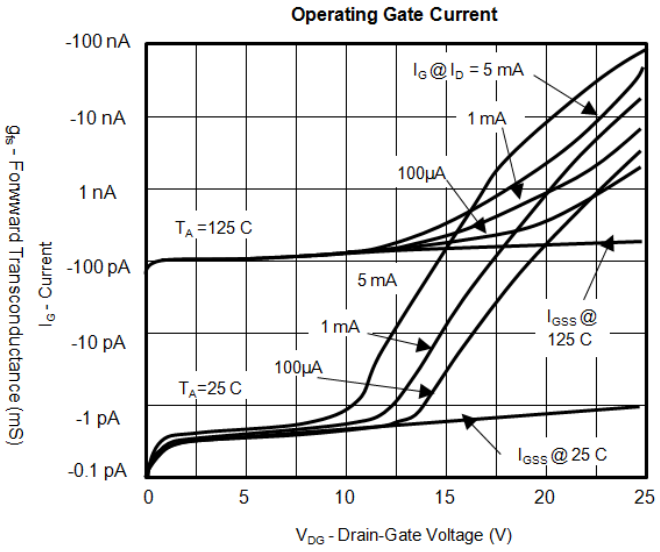
DIMENSIONS IN MILLIMETERS

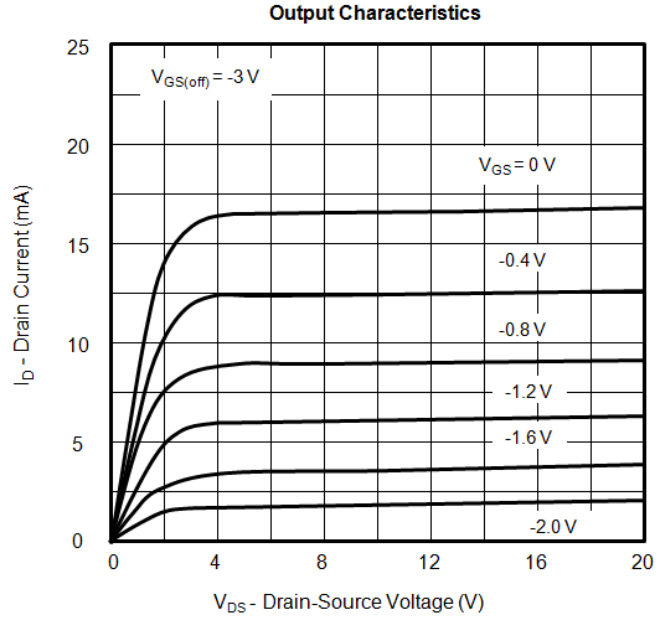
Notes:

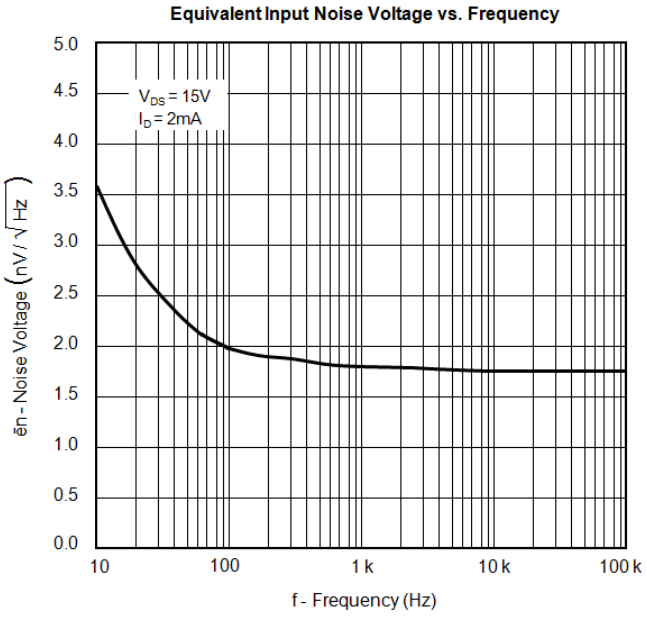
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse width ≤2$_{ms}$.
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate electrical polarity only.
4. Derate 2.4 mW/°C above 25°C.
5. Derate 4 mW/°C above 25°C.

Typical Characteristics

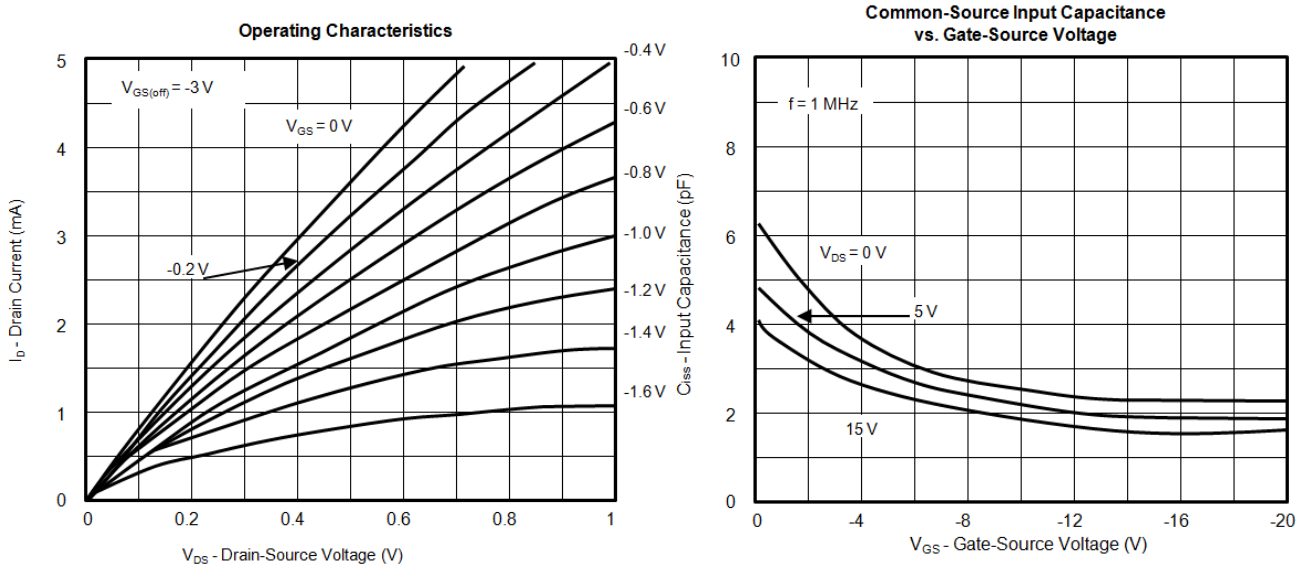


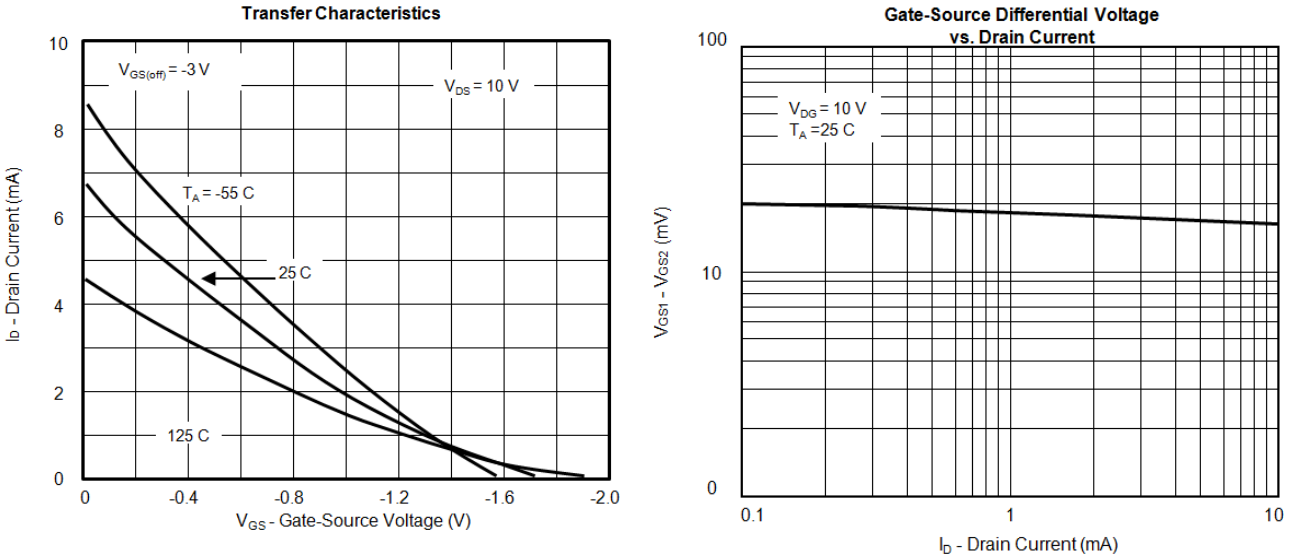






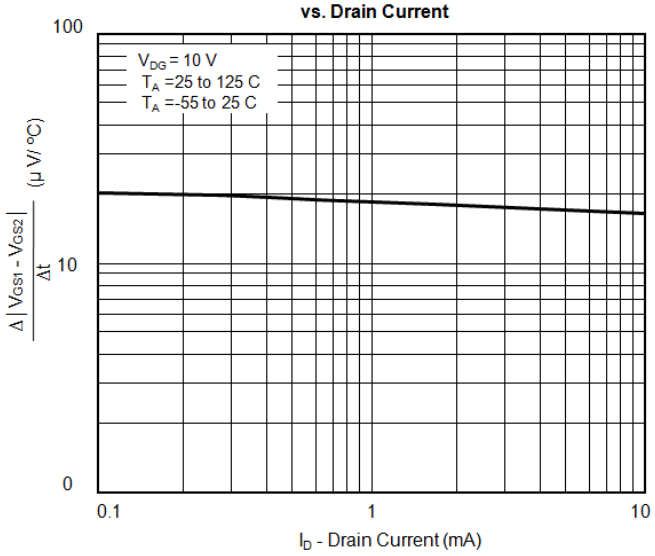
Typical Characteristics Continued



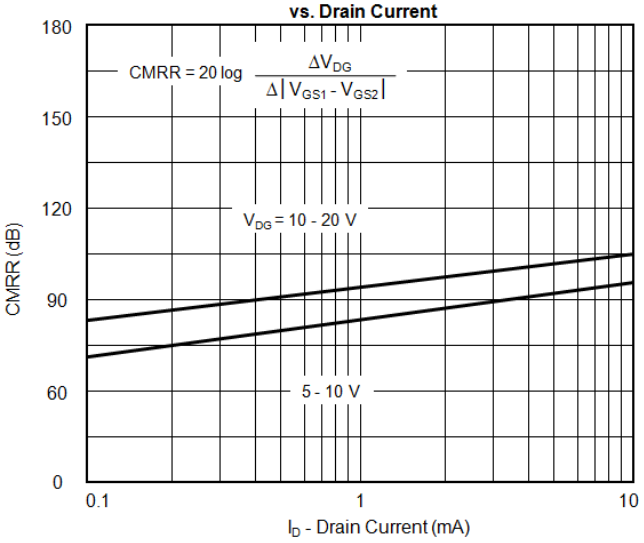


Typical Characteristics Continued

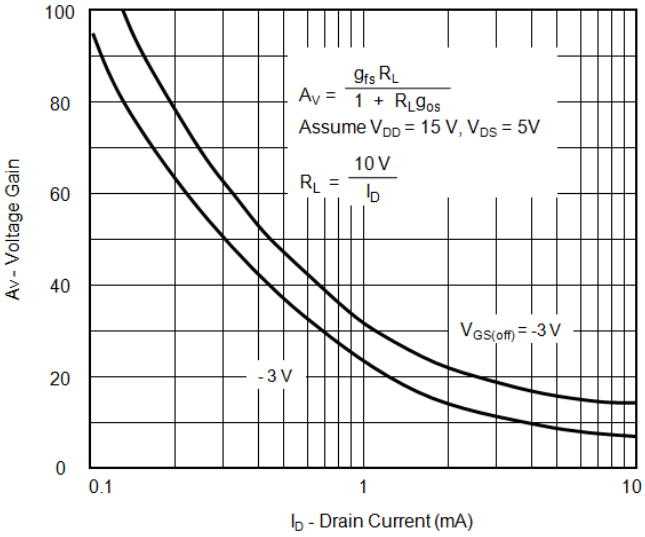
Voltage Differential with Temperature vs. Drain Current



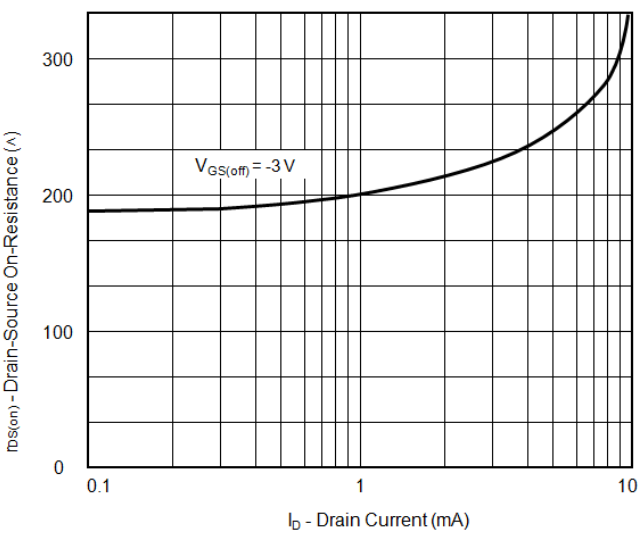
Common Mode Rejection Ration vs. Drain Current



Circuit Voltage Gain vs. Drain Current

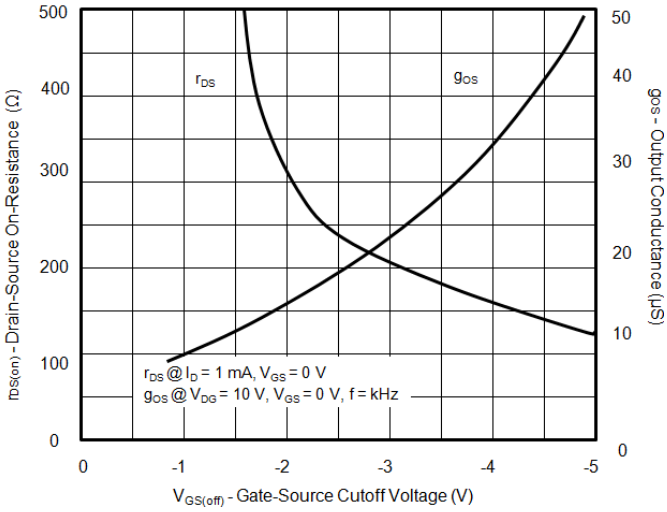


On-Resistance vs. Drain Current

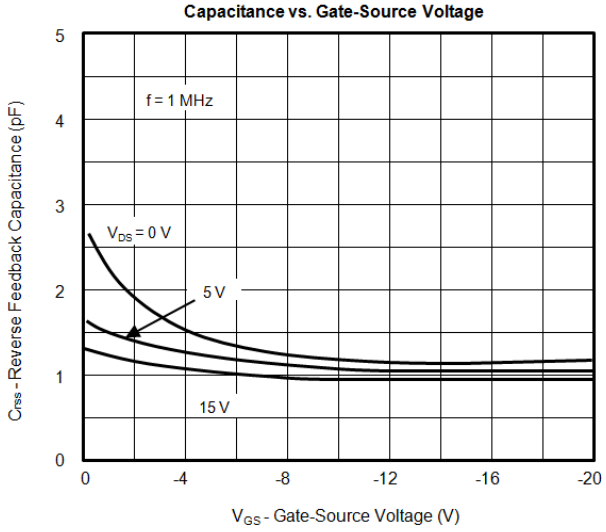


Typical Characteristics Continued

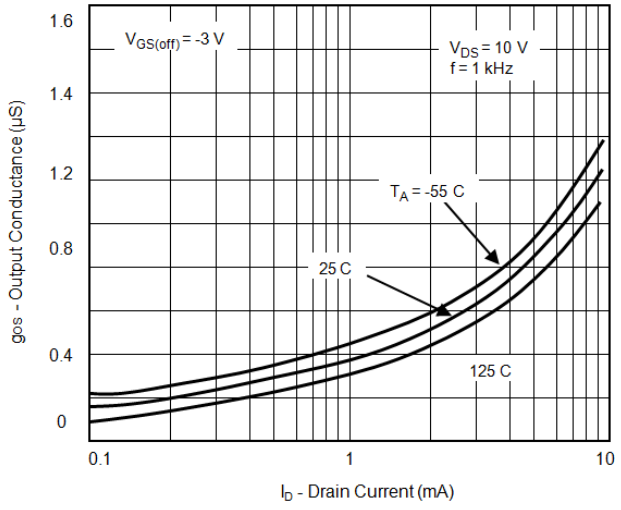
On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage



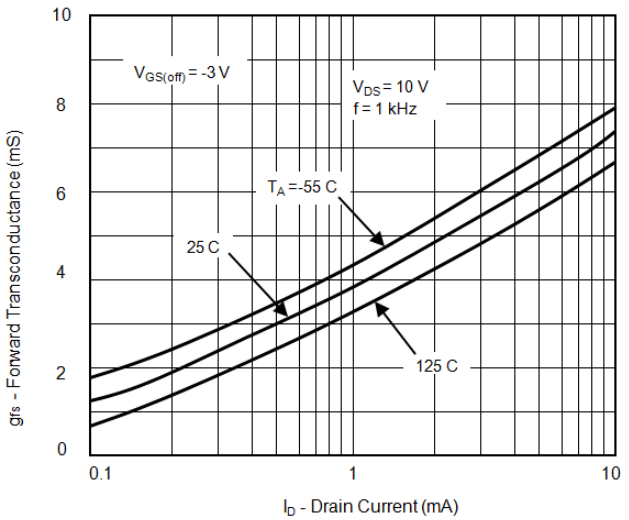
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



Output Conductance vs. Drain Current



Common-Source Forward Transconductance vs. Drain Current



LINEAR SYSTEMS

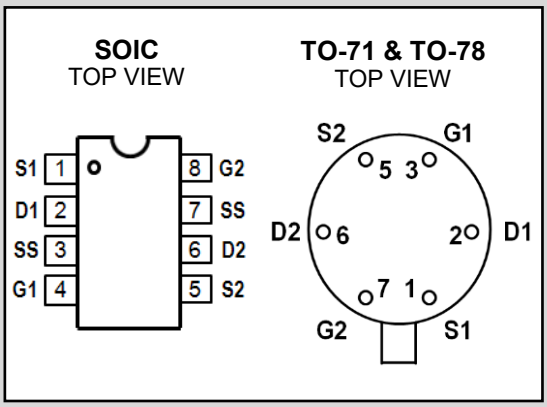
Over Three Decades of Quality Through Innovation

LS840 LS841 LS842

LOW NOISE LOW DRIFT LOW CAPACITANCE MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
LOW NOISE	e_n=8nV/Hz TYP.
LOW LEAKAGE	I_G=10pA TYP.
LOW DRIFT	I V_{GS1-2}/TI=5µV/ºC max.
LOW OFFSET VOLTAGE	IV_{GS1-2}I=2mV TYP.

ABSOLUTE MAXIMUM RATINGS[1] @ 25°C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55°C to +150°C
Operating Junction Temperature		-55°C to +150°C
Maximum Voltage and Current for Each Transistor[1]		
-V_{GSS}	Gate Voltage to Drain or Source	60V
$I_{G(f)}$	Gate Forward Current	10mA
Maximum Power Dissipation		
Device Dissipation[2] @ Free Air - Total		400mW T_A=+25°C

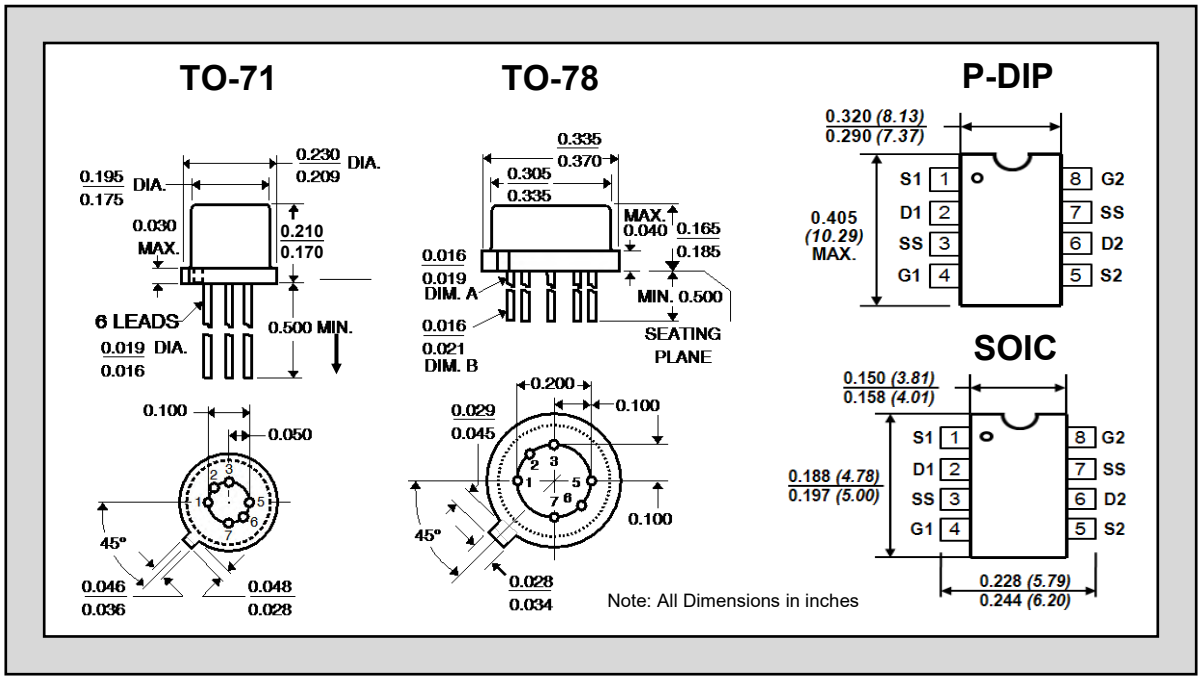


ELECTRICAL CHARACTERISTICS @ 25ºC (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS840	LS841	LS842	UNITS	CONDITIONS
I V_{GS1-2} / TI max.	Drift vs. Temperature	5	10	40	µV/ºC	V_{DG} = 20V I_D = 200µA T_A = -55ºC to +125ºC
IV_{GS1-2}I max.	Offset Voltage	5	10	25	mA	V_{DG} = 20V I_D = 200µA

SYMBOL	CHARACTERISTIC[3]	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-60	--	--	V	V_{DS}= 0 I_D= -1nA
BV_{GGO}	Gate-to-Gate Breakdown	±60	--	--	V	I_{GGO}= ±1µA I_D= 0 I_S = 0
	TRANSCONDUCTANCE					
G_{fss}	Full Conduction	1000		4000	µS	V_{DG}= 20V V_{GS}= 0 f = 1kHz
G_{fs}	Typical Conduction	500		1000	µS	V_{DG}= 20V I_D= 200µA
$\frac{G_{fs1}}{G_{fs2}}$	Transconductance Ratio	0.97		1.0		V_{DG}= 20V I_D= 200µA; Note 4
	DRAIN CURRENT					
I_{DSS}	Full Conduction	0.5	2	5	mA	V_{DG}= 20V V_{GS}= 0
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio	0.95		1.0		
	GATE-SOURCE					
V_{GS}(off)	Pinchoff Voltage	-1	-2	-4.5	V	V_{DS}= 20V I_D= 1nA
V_{GS}	Operating Range	-0.5	--	-4	V	V_{DS}= 20V I_D= 200µA
	GATE CURRENT					
-I_G	Operating	--	10	50	pA	V_{DG}= 20V I_D =200µA
-I_G	High Temperature	--	--	50	nA	V_{DG}= 20V I_D =200µA T_A=+125ºC
-I_G	Reduced VDG	--	5	--	pA	V_{DG}= 10V I_D =200µA
-I_{GSS}	At Full Conduction	--	--	100	pA	V_{DG}= 20V V_{DS} =0

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS		
	OUTPUT CONDUCTANCE							
G_{OSS}	Full Conduction	--	--	10	µS	V_{DG}= 20V	V_{GS}= 0	
G_{OS}	Operating	--	0.1	1	µS	V_{DG}= 20V	I_D= 200µA	
$\lvert G_{OS\ 1\text{-}2} \rvert$	Differential	--	0.01	0.1	µS			
	COMMON MODE REJECTION							
CMRR	-20 log $\lvert V_{GS1\text{-}2} / V_{DS} \rvert$	--	100	--	dB	V_{DS}= 10 to 20V		I_D=200µA
CMRR		--	75	--	dB	V_{DS}= 5 to 10V		I_D=200µA
	NOISE							
NF	Figure	--	--	0.5	dB	V_{DS}= 20V f= 100Hz	V_{GS}= 0 NBW= 6Hz	R_G=10M
e_n	Voltage	--	--	10	nV/Hz	V_{DS}= 20V NBW= 1Hz	I_D= 200µA	f= 1KHz
e_n	Voltage	--	--	15	nV/Hz	V_{DS}= 20V NBW= 1Hz	I_D= 200µA	f= 10Hz
	CAPACITANCE							
C_{ISS}	Input	--	4	10	pF	V_{DS}= 20V	I_D=200µA	
C_{RSS}	Reverse Transfer	--	1.2	5	pF			
C_{DD}	Drain-to-Drain	--	0.1	--	pF	V_{DG}= 20V	I_D= 200µA	



NOTES:

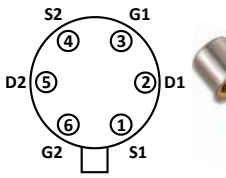
1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired
2. Derate 4mW/ºC above 25ºC
3. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicate electrical polarity only.
4. Assumes smaller number in the numerator.

LS843 Series

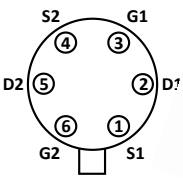
Low Noise, Monolithic Dual N-Channel JFET Amplifier

LOW INPUT CAPACITANCE MONOLITHIC DUAL N-CHANNEL JFET

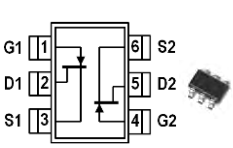
FEATURES		
Ultra-Low Noise	e_n=2.5nV/Hz @1kHz TYP.	
Low Leakage	I_G=15pA TYPs.	
Low Drift	I V_{GS1-2}/TI=5µV/ºC max.	
Ultra-Low Offset Voltage	IV_{GS1-2}I=1mV max.	
ABSOLUTE MAXIMUM RATINGS[1] @ 25°C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55º to +150°C
Operating Junction Temperature		-55º to +150°C
Maximum Voltage and Current for Each Transistor[1]		
-V_{GSS}	Gate Voltage to Drain or Source	60V
$I_{G(f)}$	Gate Forward Current	50mA
Maximum Power Dissipation[2]		
Device Dissipation[2] @ Free Air - Total		400mW T_A=+25°C



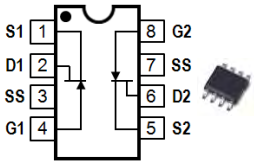
TO-71 6L
Top View



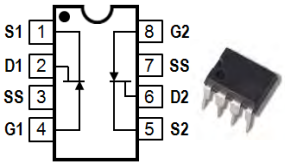
TO-78 6L
Top View



SOT-23 6L
Top View



SOIC-A 8L
Top View



PDIP 8L
Top View

* For equivalent single version, see LSK189

Features

- Low Noise: e_n = 2.5nV/√Hz (typ), *f* = 1kHz, NBW = 1Hz
- Very Low Common Source Input Capacitance of C_{ISS} = 3pF – typ and 8pF- max
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage I_{GSS} and I_G
- High CMRR 102 dB

Benefits

- Tight Differential Voltage Match vs. Current
- Improved Op Amp Speed Settling Time Accuracy
- Minimum Input Error Trimming Error Voltage
- Lower Intermodulation Distortion

Applications

- Wideband Differential Amplifiers
- High Speed Temperature Compensated Single Ended Input Amplifier Amps
- High Speed Comparators
- Impedance Converters
- Sonobouys and Hydrophones
- Acoustic Sensors

Description

The LS843 Series is the industry's lowest input capacitance and low-noise monolithic dual N-Channel JFET. Low input capacitance substantially reduces intermodulation distortion. In addition, these dual JFETs feature tight offset voltage and low drift over temperature range, and are targeted for use in a wide range of precision instrumentation and sensor applications.

The LS843 Series is available in surface mount plastic SOIC 8L, PDIP 8L and SOT-23 6L packages. Additionally, it is offered in thru-hole metal cans; the TO-71 6L and TO-78 6L package.

For an equivalent single N-Channel version refer to the LSK189 datasheet. LS843 Series TO-71 6L and SOIC 8L are fit, form and pin compatible to the same LSK389 product.

The LS843 Series provides an increase in capabilities for a wide range of low-noise applications.

The most significant aspect of the LS843 Series is how it combines a noise level comparable with the LSK389 while having much lower gate-to-drain capacitance, 4pF versus the 25pF. The slightly higher noise of the LS843 Series, versus the LSK389, is not significant in most instances, while the much lower capacitance enables designers to produce simpler, more elegant circuit designs with fewer devices that cost less in production.

Like the Linear Systems LSK389, the LS843 Series features a unique design construction of interleaving both JFETs on the same piece of silicon to provide excellent matching and thermal tracking, as well a low-noise profile having nearly zero popcorn noise.

Electrical Characteristics @ 25ºC (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS843	LS844	LS845	UNITS	CONDITIONS
I V_{GS1-2} / TI max.	Drift vs. Temperature	5	10	25	µV/ºC	V_{DG}= 10V I_D= 500µA T_A= -55ºC to +125ºC
IV_{GS1-2}I max.	Offset Voltage	1	5	15	mV	V_{GS}= 10V I_D= 500µA

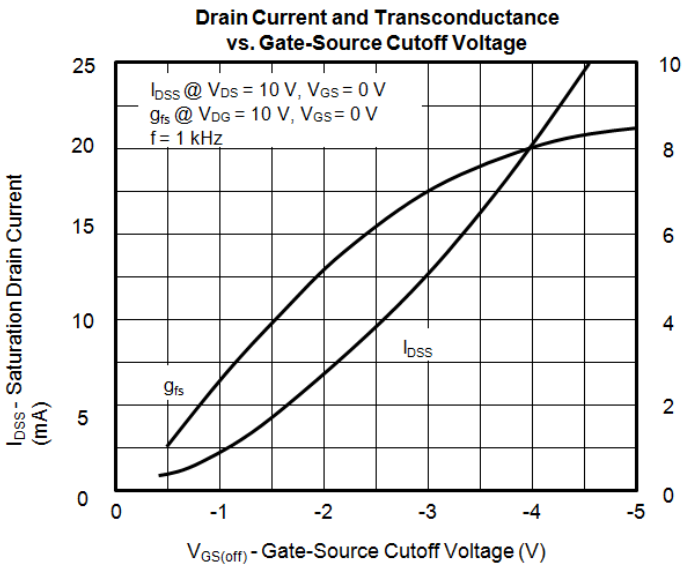
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-60	--	--	V	V_{DS}= 0 I_D= -1nA
BV_{GGO}	Gate-to-Gate Breakdown	±60	--	--	V	I_{GGO}= ±1µA I_D= 0 I_S= 0
G_{fss}	**TRANSCONDUCTANCE** Full Conduction	1500	--	--	µS	V_{DS}= 15V V_{GS}= 0 f = 1kHz
G_{fs}	Typical Conduction	1000	1500	--	µS	V_{DS}= 15V I_D= 500µA
$\lvert G_{fs1-2}/G_{fs1} \rvert$	Mismatch	--	0.6	3	%	
I_{DSS}	**DRAIN CURRENT** Full Conduction	1.5	5	15	mA	V_{DS}= 15V V_{GS}= 0
$\lvert I_{DSS1-2}/I_{DSS} \rvert$	Mismatch at Full Conduction	--	1	5	%	
V_{GS}(off)	**GATE VOLTAGE** Pinchoff Voltage	-1	--	-3.5	V	V_{DS}= 15V I_D= 1nA
V_{GS}	Operating Range	-0.5	--	-3.5	V	V_{DS}= 15V I_D= 500µA
$-I_G$	**GATE CURRENT** Operating	--	15	50	pA	V_{DG}= 15V I_D= 500µA
$-I_G$	High Temperature	--	--	50	nA	V_{DG}= 15V I_D= 500µA T_A=+125ºC
$-I_G$	Reduced VDG	--	5	30	pA	V_{DG}= 3V I_D= 500µA
$-I_{GSS}$	At Full Conduction	--	--	100	pA	V_{GS}= 15V V_{GS}= 0
G_{OSS}	**OUTPUT CONDUCTANCE** Full Conduction	--	--	40	µS	V_{DS}= 15V V_{GS}= 0
G_{OS}	Operating	--	2.0	2.7	µS	V_{DS}= 15V I_D= 200µA
$\lvert G_{OS\ 1-2} \rvert$	Differential	--	0.02	0.2	µS	

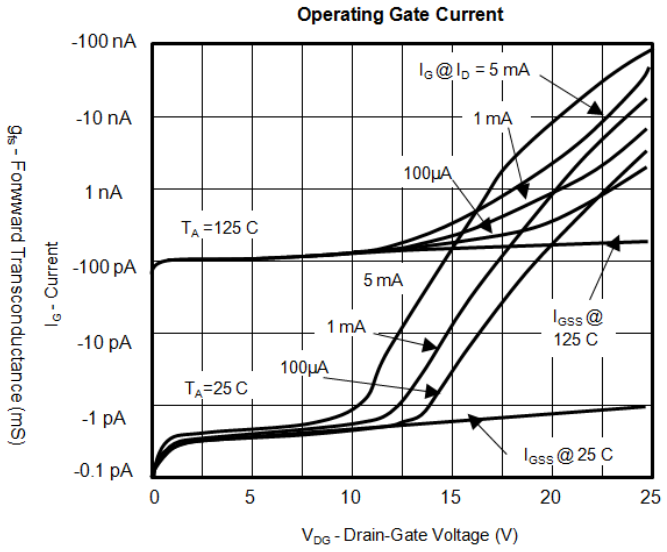
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	COMMON MODE REJECTION					
CMRR	-20 log $\lvert \Delta V_{GS1-2} / \Delta V_{DS} \rvert$	90	100	--	dB	V_{DS}= 10 to 20V I_D= 500µA
CMRR		--	85	--	dB	V_{DS}= 5 to 10V I_D= 500µA
NF	**NOISE** Figure	--	--	0.5	dB	V_{DS}= 15V V_{GS}= 0 R_G= 10MΩ f= 100Hz NBW= 6Hz
e_n	Voltage	--	--	7	nV/Hz	V_{DS}= 15V I_D= 500µA f= 1kHz NBW= 1Hz
e_n	Voltage	--	--	11	nV/Hz	V_{DS}= 15V I_D= 500µA f= 10Hz NBW= 1Hz
C_{ISS}	**CAPACITANCE** Input	--	--	8	pF	V_{DS}= 15V I_D= 500µA f= 1mHz
C_{RSS}	Reverse Transfer	--	--	3	pF	
C_{DD}	Drain-to-Drain	--	0.5	--	pF	V_{DD}= 15V I_D= 500µA f= 1mHz

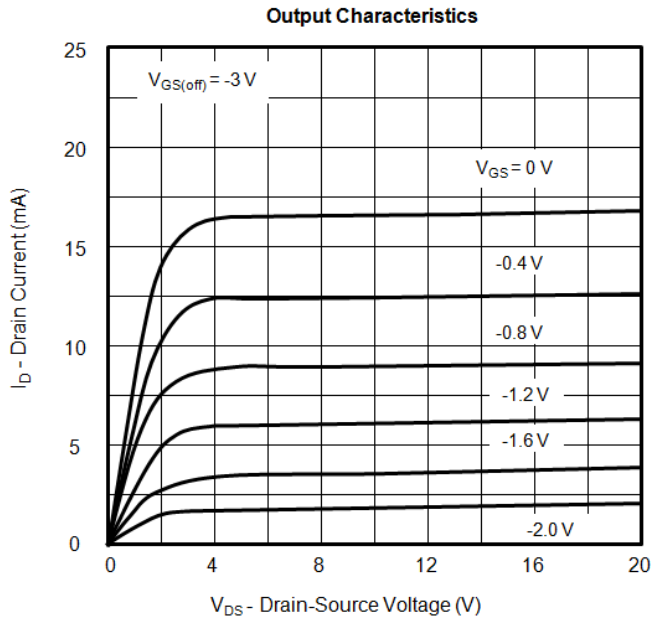
Notes:

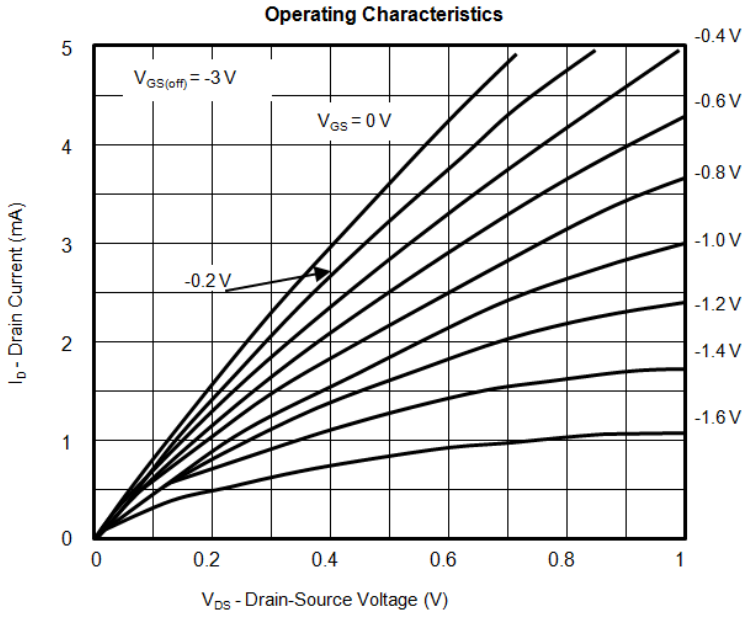
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse width ≤2ms.
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate electrical polarity only.
4. Derate 2.4 mW/°C above 25°C.
5. Derate 4 mW/°C above 25°C.

Typical Characteristics



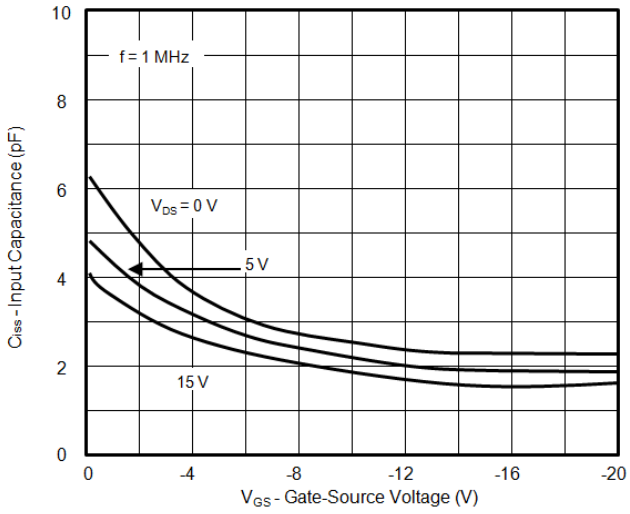




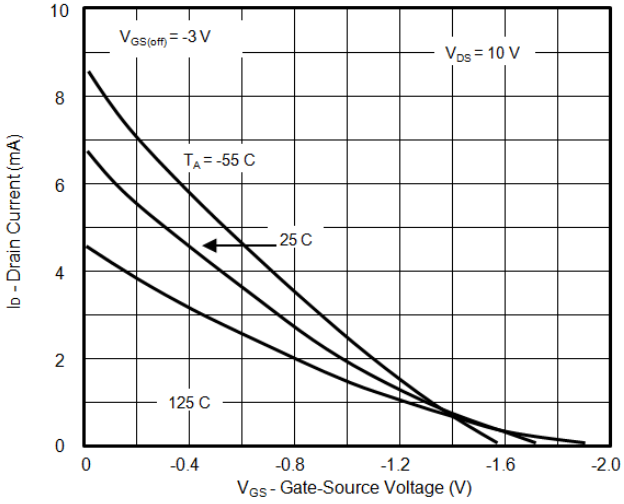


Typical Characteristics Continued

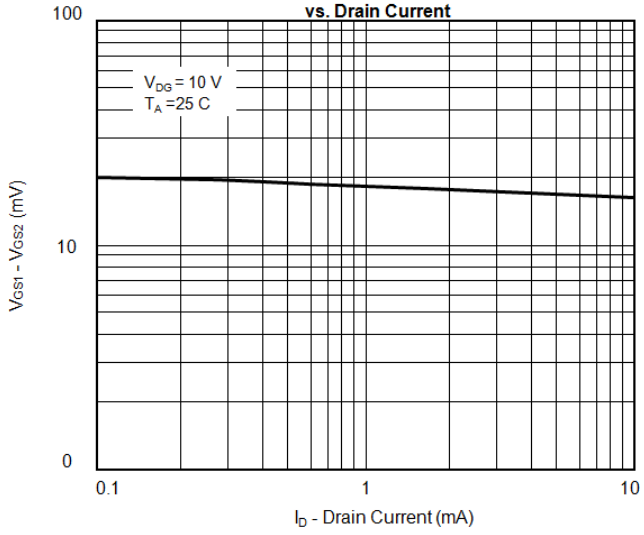
Common-Source Input Capacitance vs. Gate-Source Voltage



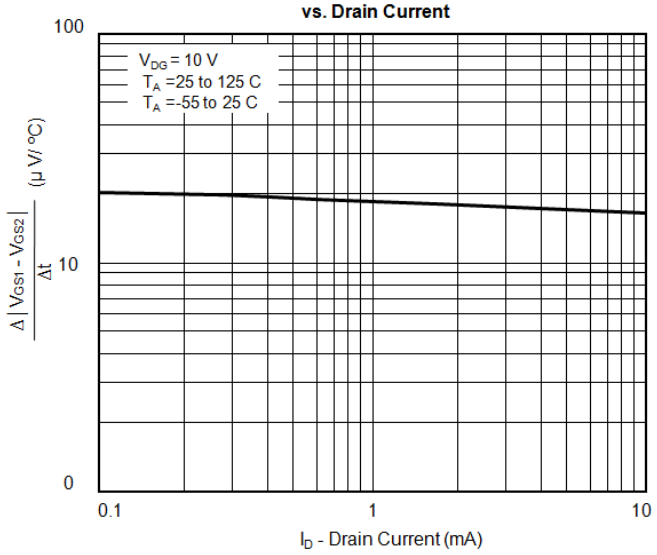
Transfer Characteristics



Gate-Source Differential Voltage vs. Drain Current

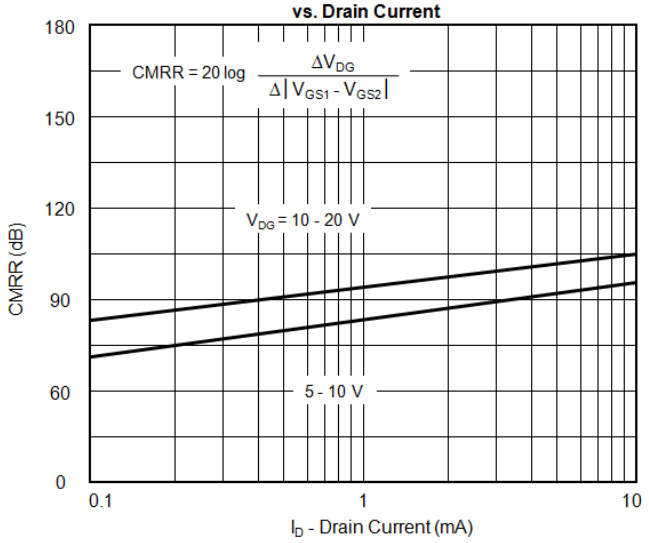


Voltage Differential with Temperature vs. Drain Current

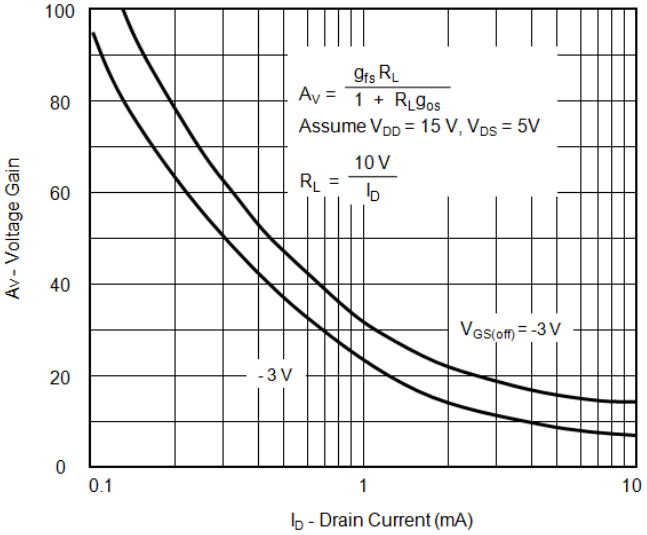


Typical Characteristics Continued

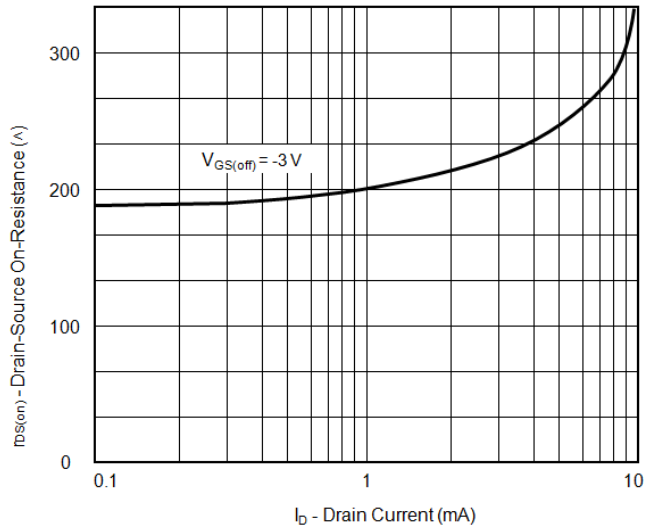
Common Mode Rejection Ration vs. Drain Current



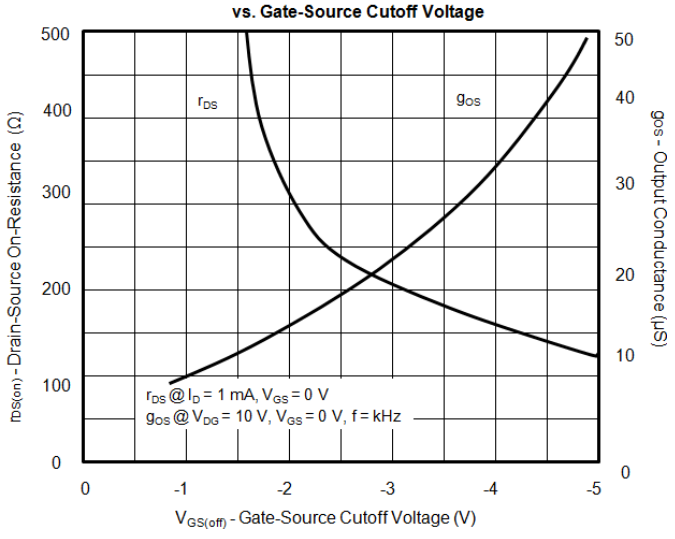
Circuit Voltage Gain vs. Drain Current



On-Resistance vs. Drain Current

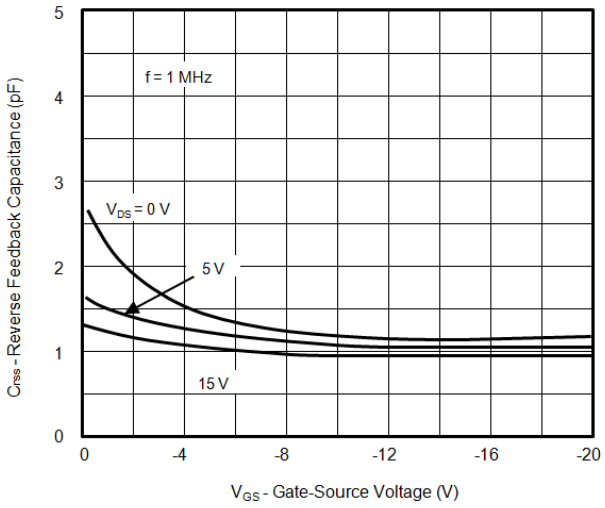


On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage

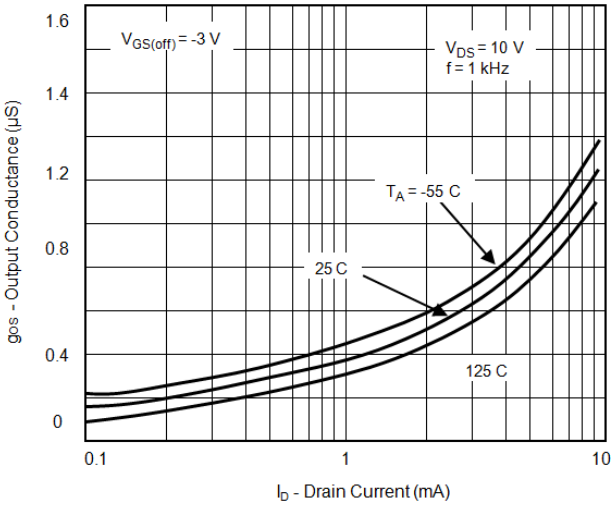


Typical Characteristics Continued

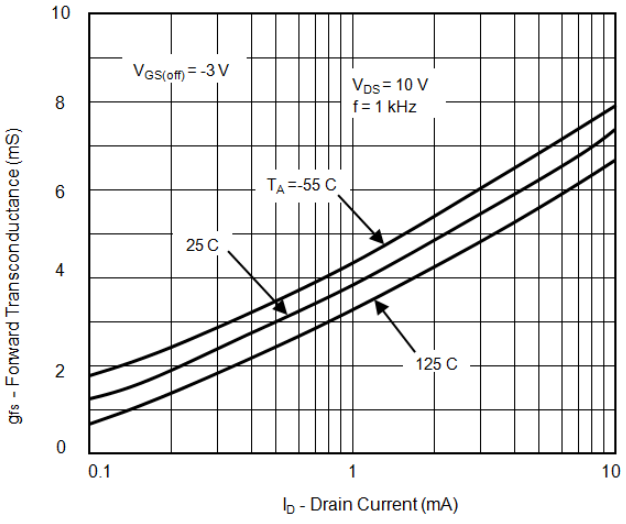
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



Output Conductance vs. Drain Current

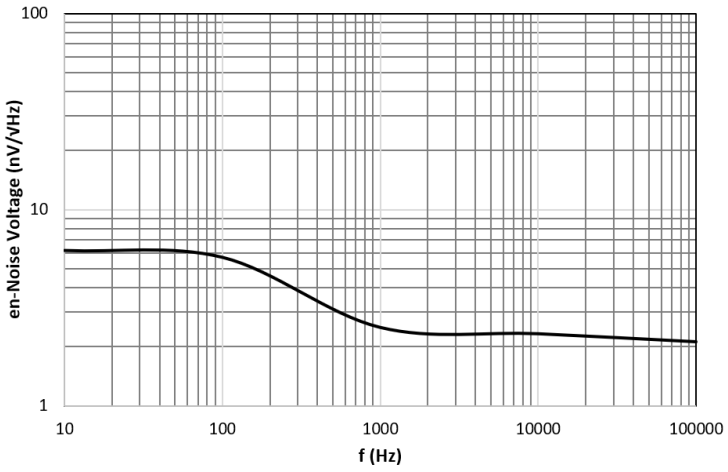


Common-Source Forward Transconductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency

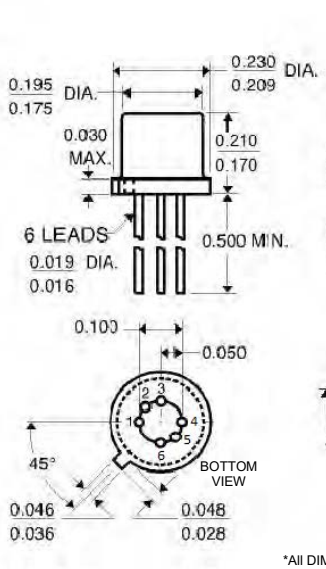
VDS=15V
ID=2mA



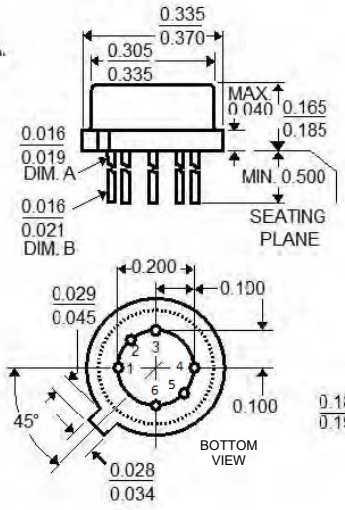
LS843 Series

Package Dimensions:

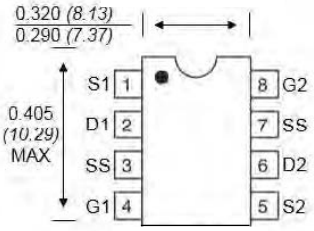
TO-71
6 Lead



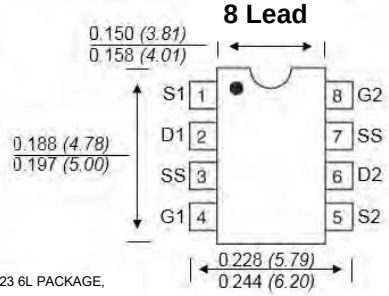
TO-78
6 Lead



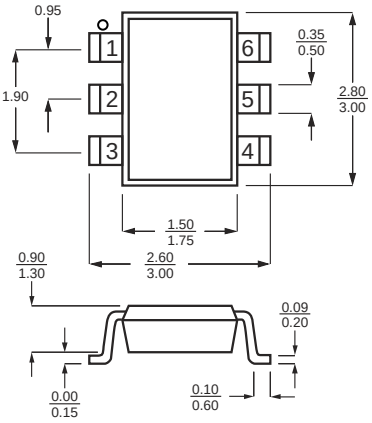
PDIP
8 Lead



SOIC
8 Lead



SOT-23
6 Lead



*All DIMENSIONS IN INCHES EXCEPT FOR THE SOT-23 6L PACKAGE, WHICH IS IN MILLIMETERS

Ordering Information:

Standard Part Call-Out		
LS843 TO-71 6L RoHS	LS844 TO-71 6L RoHS	LS845 TO-71 6L RoHS
LS843 TO-78 6L RoHS	LS844 TO-78 6L RoHS	LS845 TO-78 6L RoHS
LS843 SOT-23 6L RoHS	LS844 SOT-23 6L RoHS	LS845 SOT-23 6L RoHS
LS843 SOIC 8L RoHS	LS844 SOIC 8L RoHS	LS845 SOIC 8L RoHS
LS843 PDIP 8L RoHS	LS844 PDIP 8L RoHS	LS845 PDIP 8L RoHS
Custom Part Call-Out (Custom Parts Include SEL + 4 Digit Numeric Code)		
LS843 TO-71 6L RoHS SELXXXX	LS844 TO-71 6L RoHS SELXXXX	LS845 TO-71 6L RoHS SELXXXX
LS843 TO-78 6L RoHS SELXXXX	LS844 TO-78 6L RoHS SELXXXX	LS845 TO-78 6L RoHS SELXXXX
LS843 SOT-23 6L RoHS SELXXXX	LS844 SOT-23 6L RoHS SELXXXX	LS845 SOT-23 6L RoHS SELXXXX
LS843 SOIC 8L RoHS SELXXXX	LS844 SOIC 8L RoHS SELXXXX	LS845 SOIC 8L RoHS SELXXXX
LS843 PDIP 8L RoHS SELXXXX	LS844 PDIP 8L RoHS SELXXXX	LS845 PDIP 8L RoHS SELXXXX

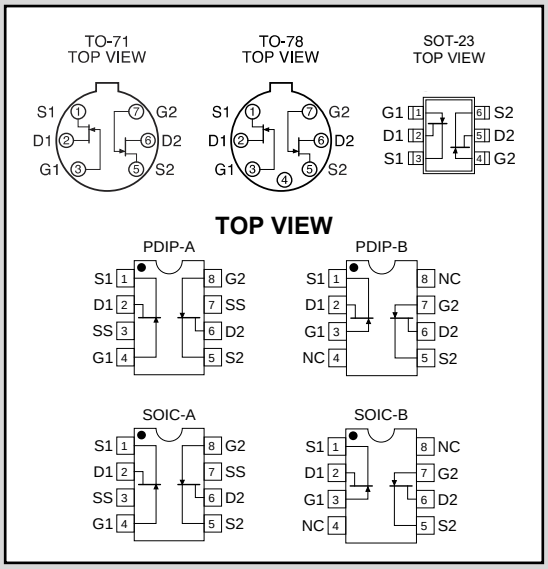
LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

LS5911 LS5912 LS5912C

IMPROVED LOW NOISE WIDEBAND MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
Improved Replacement for SILICONIX, FAIRCHILD, & NATIONAL: 2N5911 & 2N5912	
LOW NOISE (10kHz)	e_n ~ 4nV/√Hz
HIGH TRANSCONDUCTANCE (100MHz)	g_{fs} ≥ 4000µS
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Maximum Power Dissipation	
Continuous Power Dissipation (Total)[4]	500mW
Maximum Currents	
Gate Current	50mA
Maximum Voltages	
Gate to Drain	-25V
Gate to Source	-25V



MATCHING ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	TYP	LS5911		LS5912		LS5912C		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate to Source Cutoff Voltage			10		15		40	mV	V_{DG} = 10V, I_D = 5mA
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Differential Gate to Source Voltage Change with Temperature			20		40		40	µV/°C	V_{DG} = 10V, I_D = 5mA T_A = -55 to +125°C
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio		0.95	1	0.95	1	0.95	1		V_{DS} = 10V, V_{GS} = 0V Notes 2, 3
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current			20		20		20	nA	V_{DG} = 10V, I_D = 5mA T_A = +125°C
$\frac{g_{fs1}}{g_{fs2}}$	Forward Transconductance Ratio		0.95	1	0.95	1	0.95	1		V_{DS} = 10V, I_D = 5mA *f* = 1kHz[3]
CMRR	Common Mode Rejection Ratio	85							dB	V_{DG} = 5V to 10V I_D = 5mA

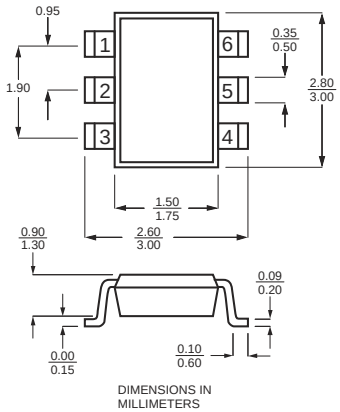
STATIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	LS5911		LS5912		LS5912C		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown		-25		-25		-25		V	I_G = -1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage		-1	-5	-1	-5	-1	-5		V_{DS} = 10V, I_D = 1nA
$V_{GS(F)}$	Gate to Source Forward Voltage	0.7								I_G = 1mA, V_{DS} = 0V
V_{GS}	Gate to Source Voltage		-0.3	-4	-0.3	-4	-0.3	-4		V_{DG} = 10V, I_G = 5mA
I_{DSS}	Drain to Source Saturation		7	40	7	40	7	40	mA	V_{DS} = 10V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current	-1		-50		-50		-50	pA	V_{GS} = -15V, V_{DS} = 0V
I_G	Gate Operating Current	-1		-50		-50		-50		V_{DG} = 10V, I_D = 5mA
IG1G2	Gate to Gate Isolation Current			±1		±1		±1	uA	V_{G1}-V_{G2}=±25VI_D = I_S = 0

DYNAMIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

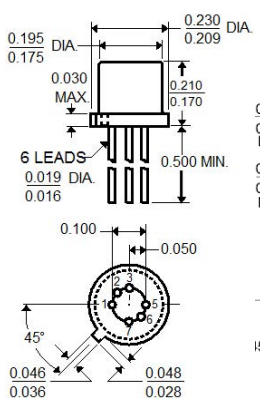
SYM.	CHARACTERISTIC		TYP	LS5911		LS5912		LS5912C		UNIT	CONDITIONS
				MIN	MAX	MIN	MAX	MIN	MAX		
g_{fs}	Forward Transconductance	f = 1kHz		4000	10000	4000	10000	4000	10000	μS	V_{DG} = 10V, I_D = 5mA
		f = 100MHz	7000								
g_{os}	Output Conductance	f = 1kHz			100		100		100		
		f = 100MHz	120								
C_{iss}	Input Capacitance				5		5		5	pF	V_{DG} = 10V, I_D = 5mA f = 1MHz
C_{rss}	Reverse Transfer Capacitance				1.2		1.2		1.2		
NF	Noise Figure				1		1		1	dB	V_{DG} = 10V, I_D = 5mA f = 10kHz, R_G = 100KΩ
e_n	Equivalent Input Noise Voltage	f = 100Hz	7		20		20		20	nV/√Hz	V_{DG} = 10V, I_D = 5mA f = 100Hz
		f = 10kHz	4		10		10		10	nV/√Hz	V_{DG} = 10V, I_D = 5mA f = 10kHz

SOT-23

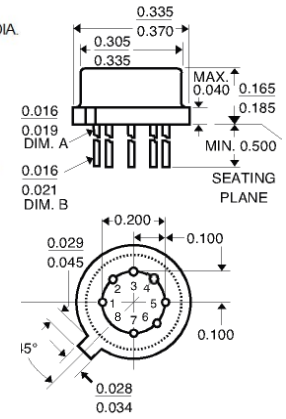


DIMENSIONS IN MILLIMETERS

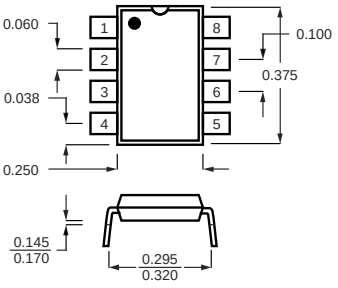
TO-71



TO-78

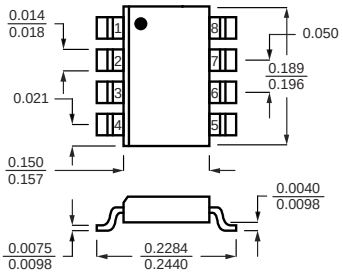


PDIP



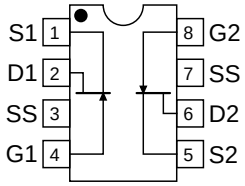
DIMENSIONS IN INCHES

SOIC

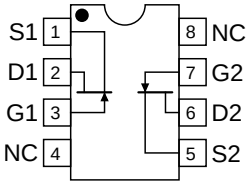


DIMENSIONS IN INCHES

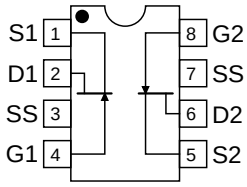
PDIP-A



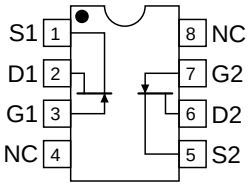
PDIP-B



SOIC-A



SOIC-B



Please contact the factory regarding the availability of optional packages.

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300μs Duty Cycle ≤ 3%
3. Assumes smaller value in numerator.
4. Derate 4mW/°C above 25°C.

LINEAR SYSTEMS

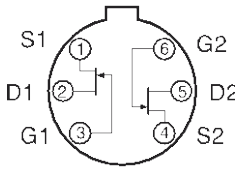
Improved Standard Products®

U/SST440, 441

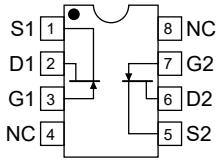
WIDEBAND HIGH GAIN MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
Direct Replacement for SILICONIX U/SST440 & U/SST441	
HIGH CMRR	CMRR ≥ 85dB
LOW GATE LEAKAGE	I_{GSS} ≤ 1pA
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Maximum Power Dissipation @ TA = 25°C	
Continuous Power Dissipation (Total)	500mW
Maximum Currents	
Gate Current	50mA
Maximum Voltages	
Gate to Drain	-25V
Gate to Source	-25V
Gate to Gate	±50V

U SERIES TO-71 TOP VIEW



SST SERIES SOIC TOP VIEW



MATCHING CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate to Source Cutoff Voltage	U/SST440			10	mV	V_{DG} = 10V, I_D = 5mA
		U/SST441			20		
$\frac{\Delta\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Differential Gate to Source Cutoff Voltage Change with Temperature			20		µV/°C	V_{DG} = 10V, I_D = 5mA T_A = -55 to +125°C
$\frac{I_{DSS1}}{I_{DSS2}}$	Gate to Source Saturation Current Ratio[3]			0.98			V_{DS} = 10V, V_{GS} = 0V
$\frac{g_{fs1}}{g_{fs2}}$	Forward Transconductance Ratio[2]			0.97			V_{DS} = 10V, I_D = 5mA, *f* = 1kHz
CMRR	Common Mode Rejection Ratio			85		dB	V_{DG} = 5 to 10V, I_D = 5mA

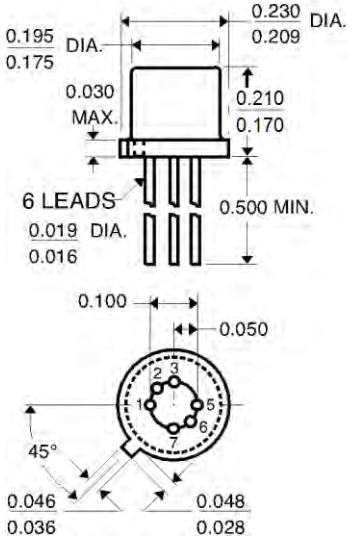
ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-25			V	I_G = -1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-1	-3.5	-6	V	V_{DS} = 10V, I_D = 1nA
I_{DSS}	Gate to Source Saturation Current[2]	6	15	30	mA	V_{DS} = 10V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current		-1	-500	pA	V_{GS} = -15V, V_{DS} = 0V
I_G	Gate Operating Current		-1	-500		V_{DG} = 10V, I_D = 5mA

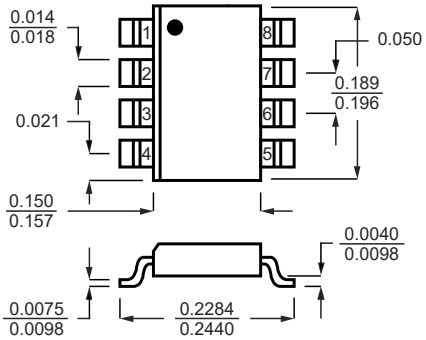
ELECTRICAL CHARACTERISTICS CONTINUED @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
g_{fs}	Forward Transconductance	4.5	6	9	mS	V_{DS} = 10V, I_D = 5mA, *f* = 1kHz
g_{os}	Output Conductance		70	200	µS	
C_{iss}	Input Capacitance		3		pF	V_{DS} = 10V, I_D = 5mA, *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance		1			
e_n	Equivalent Input Noise Voltage		4		nV/√Hz	V_{DS} = 10V, I_D = 5mA, *f* = 10kHz

TO-71
Six Lead



SOIC



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs Duty Cycle ≤ 3%
3. Assumes smaller value in numerator.

LINEAR SYSTEMS

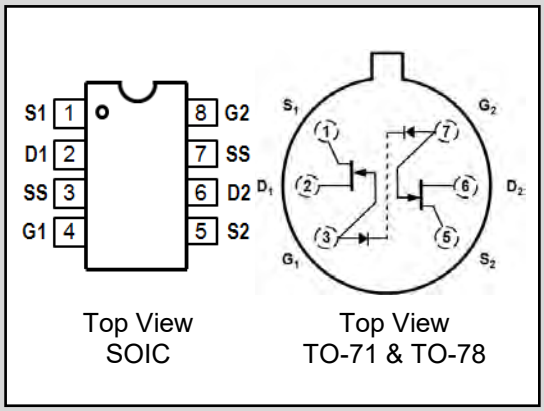
Over 30 Years of Quality Through Innovation

LS830 LS831 LS832 LS833

ULTRA LOW LEAKAGE LOW DRIFT MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
ULTRA LOW DRIFT	$\lvert \Delta V_{GS1-2}/\Delta T \rvert$ = 5µV/ºC max.
ULTRA LOW NOISE	I_G=80fA TYP.
LOW NOISE	e_n=70nV/√Hz TYP.
LOW CAPACITANCE	C_{ISS}=3pf max.

ABSOLUTE MAXIMUM RATINGS NOTE 1 @ 25°C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55 to +150°C
Operating Junction Temperature		-55 to +150°C
Maximum Voltage and Current for Each Transistor NOTE 1		
$-V_{GSS}$	Gate Voltage to Drain or Source	40V
$-V_{DSO}$	Drain to Source Voltage	40V
$-I_{G(f)}$	Gate Forward Current	10mA
$-I_G$	Gate Reverse Current	10µA
Maximum Power Dissipation @ TA = 25ºC		
Continuous Power Dissipation (Total)		500mW



Top View SOIC

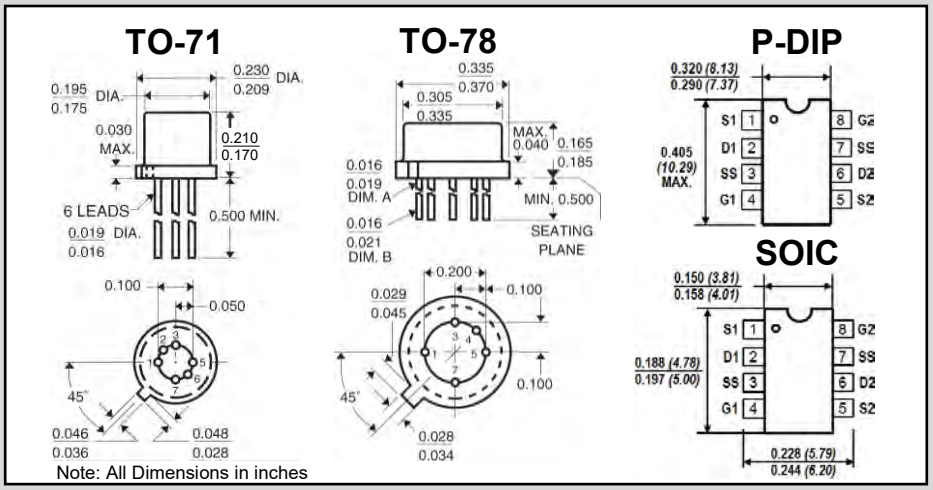
Top View TO-71 & TO-78

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-40	-60	--	V	V_{DS}= 0 I_G= -1nA
BV_{GGO}	Gate-to-Gate Breakdown	±40	--	--	V	I_G= ±1µA I_D= 0 I_S = 0
	TRANSCONDUCTANCE					
g_{fss}	Full Conduction	70	300	500	µS	V_{DG}= 10V V_{GS}= 0 f = 1kHz
g_{fs}	Typical Operation	50	100	200	µS	V_{DG}= 10V I_D= 30µA f = 1kHz
$\lvert g_{fs1-2}/g_{fs} \rvert$	Differential	--	1	5	%	
	DRAIN CURRENT					
I_{DSS}	Full Conduction	60	400	1000	µA	V_{DG}= 10V V_{GS}= 0
$\lvert I_{DSS1-2}/I_{DSS} \rvert$	Differential at Full Conduction	--	2	5	%	

ELECTRICAL CHARACTERISTICS TA = 25ºC (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS830	LS831	LS832	LS833	UNITS	CONDITIONS
$\lvert \Delta V_{GS1-2}/\Delta T \rvert$ max.	Drift vs. Temperature	5	10	20	75	µV/ºC	V_{DG} = 10V I_D = 30µA T_A = -55ºC to +125ºC
$\lvert V_{GS1-2} \rvert$ max.	Offset Voltage	25	25	25	25	mV	V_{DG} = 10V I_D = 30µA
$-I_G$ typical	Operating	0.1	0.1	0.1	0.5	pA	
$-I_G$ typical	High Temperature	0.1	0.1	0.1	0.5	nA	TA= +125ºC
I_{GSS} typical	At Full Conduction	0.2	0.2	0.2	1.0	pA	V_{GS} = 20V, V_{GS} = 0V
I_{GSS} typical	High Temperature	0.5	0.5	0.5	1.0	nA	V_{GS} = 0 V_{GS} = 20V TA= +125ºC

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS		
	GATE-SOURCE							
$V_{GS}(off)$	Cutoff Voltage	-0.6	-2	-4.5	V	V_{DS}= 10V	I_D= 1nA	
V_{GS}	Operating Range	--	--	-4	V	V_{DG}= 10V	I_D= 30µA	
	GATE CURRENT							
I_{GGO}	Gate-to-Gate Leakage	--	1	--	pA	V_{GG}= ±20V	$I_D = I_S$ = 0A	
	OUTPUT CONDUCTANCE							
g_{OSS}	Full Conduction	--	--	5	µS	V_{DG}= 10V	V_{GS}= 0	
g_{OS}	Operating	--	--	0.5	µS	V_{DG}= 10V	I_D= 30µA	
$\lvert g_{OS\ 1\text{-}2} \rvert$	Differential	--	--	0.1	µS			
	COMMON MODE REJECTION							
CMRR	-20 log $\lvert \Delta V_{GS1\text{-}2} / \Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 10 to 20V		I_D=30µA
CMRR	-20 log $\lvert \Delta V_{GS1\text{-}2} / \Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 5 to 10V		I_D=30µA
	NOISE							
NF	Figure	--	--	1	dB	V_{DS}= 10V f= 100Hz	V_{GS}= 0 NBW= 6Hz	R_G=10MΩ
e_n	Voltage	--	20	70	nV/√Hz	V_{DG}= 10V NBW= 1Hz	I_D= 30µA	f= 10Hz
	CAPACITANCE							
C_{ISS}	Input	--	--	3	pF	V_{DS}= 10V	V_{GS}= 0	f= 1MHz
C_{RSS}	Reverse Transfer	--	--	1.5	pF	V_{DS}= 10V	V_{GS}= 0	f= 1MHz
C_{DD}	Drain-to-Drain	--	--	0.1	pF	V_{DG}= 10V	I_D= 30µA	



Note: All Dimensions in inches

NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired

LINEAR SYSTEMS

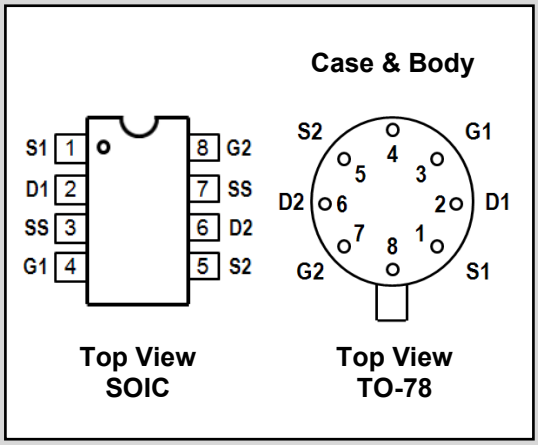
Improved Standard Products®

LS5905 LS5906 LS5907 LS5908 LS5909

LOW LEAKAGE LOW DRIFT MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
LOW DRIFT	$\lvert\Delta V_{GS1-2}/\Delta T\rvert$ =5µV/°C max.
ULTRA LOW LEAKAGE	I_G=150fA TYP.
LOW PINCHOFF	V_P=2V TYP.

ABSOLUTE MAXIMUM RATINGS[1] @ 25°C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55 to +150°C
Operating Junction Temperature		-55 to +150°C
Maximum Voltage and Current for Each Transistor[1]		
$-V_{GSS}$	Gate Voltage to Drain or Source	40V
$-I_{G(f)}$	Gate Forward Current	10mA
$-I_G$	Gate Reverse Current	10µA
Maximum Power Dissipation		
Device Dissipation @ TA=25ºC - Total		500mW[2]

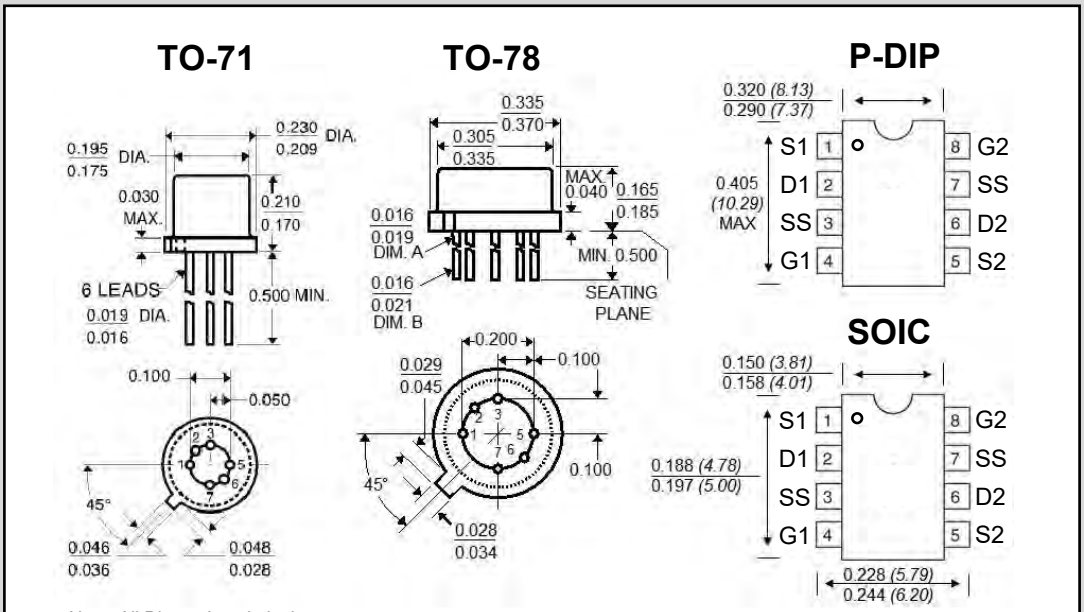


ELECTRICAL CHARACTERISTICS @ 25ºC (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS5906	LS5907	LS5908	LS5909	LS5905	UNITS	CONDITIONS
$\lvert\Delta V_{GS1-2}/\Delta T\rvert$ max.	Drift vs. Temperature	5	10	20	40	40	µV/ºC	V_{DG} = 10V, I_D=30µA T_A = -55ºC to +125ºC
$\lvert V_{GS1-2}\rvert$ max.	Offset Voltage	5	5	10	15	15	mV	V_{DG} =10V I_D=30µA
$-I_G$ Max	Operating	1	1	1	1	3	pA	
$-I_G$ Max	High Temperature	1	1	1	1	3	nA	T_A=+125 ºC
$-I_{GSS}$ Max	Gate Reverse Current	2	2	2	2	5	pA	V_{DS}=0V V_{GS}=-20V
$-I_{GSS}$ Max	Gate Reverse Current	5	5	5	5	10	nA	T_A=+125 ºC

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-40	-60	--	V	V_{DS}= 0 I_D= -1µA
BV_{GGO}	Gate-to-Gate Breakdown	±40	--	--	V	I_{GG}= ±1µA I_D= 0 I_S= 0
	TRANSCONDUCTANCE					
G_{fss}	Full Conduction	70	300	500	µS	V_{DG}= 10V V_{GS}= 0 f = 1kHz
G_{fs}	Typical Operation	50	100	200	µS	V_{DG}= 10V I_D= 30µA f = 1kHz
$\lvert G_{fs1}/G_{fs2}$[3]$\rvert$	Transconductance Ratio	--	1	5	%	
	DRAIN CURRENT					
I_{DSS}	Full Conduction	60	400	1000	µA	V_{DG}= 10V V_{GS}= 0
$\lvert I_{DSS1}/I_{DSS2}$[3]$\rvert$	Drain Current Ratio	--	2	5	%	
	GATE VOLTAGE					
V_{GS}(off)	Gate-Source Cutoff Voltage	-0.6	-2	-4.5	V	V_{DS}= 10V I_D= 1nA
V_{GS}	Operating Range	--	--	-4	V	V_{DS}= 10V I_D= 30µA
	GATE CURRENT					
I_{GGO}	Gate-to-Gate Leakage	--	±1	--	pA	V_{GG}= 20V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	OUTPUT CONDUCTANCE					
g_{oss}	Full Conduction	--	--	5	µS	V_{DG}= 10V V_{GS}= 0
g_{os}	Operating	--	0.1	--	µS	V_{DG}= 10V I_D= 30µA
$\lvert g_{os1-2} \rvert$	Differential	--	0.01	0.2	µS	
	COMMON MODE REJECTION					
CMRR	-20 log $\lvert \Delta V_{GS1-2}/\Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 10 to 20V I_D=30µA
CMRR	-20 log $\lvert \Delta V_{GS1-2}/\Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 5 to 10V I_D=30µA
	NOISE					
NF	Figure	--	--	1	dB	V_{DS}= 10V V_{GS}= 0 R_G=10MΩ f= 100Hz NBW=6Hz
e_n	Voltage	--	20	70	nV/√Hz	V_{DS}= 10V I_D= 30µA f= 10Hz NBW=1Hz
	CAPACITANCE					
C_{ISS}	Input	--	--	3	pF	V_{DS}= 10V V_{GS}= 0 f= 1MHz
C_{RSS}	Reverse Transfer	--	--	1.5	pF	V_{DS}= 10V V_{GS}= 0 f= 1MHz
C_{DD}	Drain-to-Drain	--	--	0.1	pF	V_{DG}= 20V I_D= 30µA f= 1MHz



Note: All Dimensions in inches

NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. Derate 4mWºC above 25ºC
3. Assume smaller value in the numerator.

LINEAR SYSTEMS

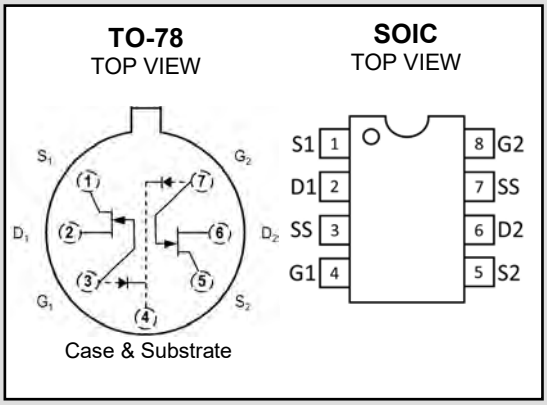
Improved Standard Products®

U421, U422, U423, U424, U425, U426

LOW LEAKAGE LOW DRIFT MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
HIGH INPUT IMPEDANCE	I_G=0.25pA MAX
HIGH GAIN	gfs=120µS MIN
LOW POWER OPERATION	$V_{GS(off)}$=2V MAX

ABSOLUTE MAXIMUM RATINGS NOTE 1 @ 25 °C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55 to +150°C
Operating Junction Temperature		-55 to +150°C
Maximum Voltage and Current for Each Transistor NOTE 1		
$-V_{GSS}$	Gate Voltage to Drain or Source	40V
$-V_{DSO}$	Drain to Source Voltage	40V
$I_{G(f)}$	Gate Forward Current	10mA
Maximum Power Dissipation		
Total Device Dissipation TA = 25ºC		500[2] mW

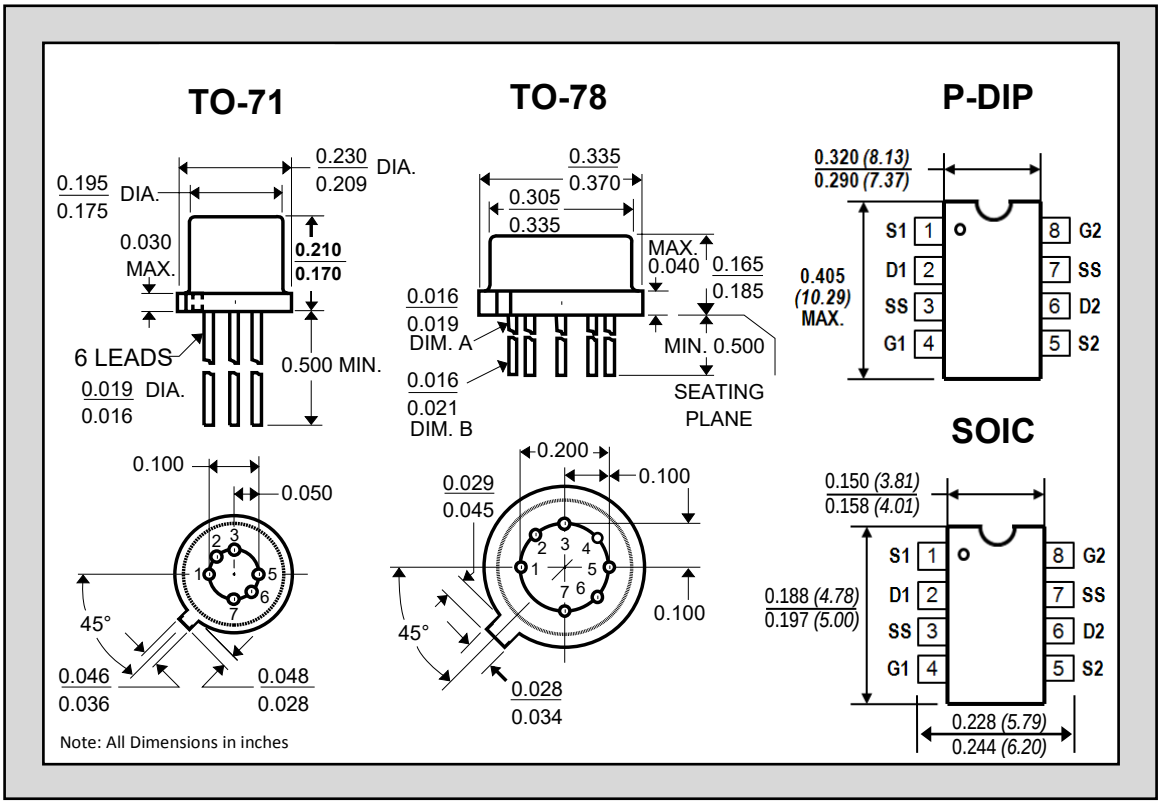


ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC[3]		U421	U422	U423	U424	U425	U426	UNITS	CONDITIONS
$\lvert\Delta V_{GS1-2}/\Delta T\rvert$ max.	Drift vs. Temperature		10	25	40	10	25	40	µV/ºC	V_{DG} = 10V I_D = 30µA T_A = -55ºC to +125ºC
$\lvert V_{GS1-2}\rvert$ max.	Offset Voltage		10	15	25	10	15	25	mV	V_{DG} =10V I_D = 30µA
	GATE VOLTAGE									
$V_{GS(off)}$	Pinchoff Voltage	Max	-2.0	-2.0	-2.0	-3.0	-3.0	-3.0	V	V_{DS}=10V I_D=1nA
		Min	-0.4	-0.4	-0.4	-0.4	-0.4	-0.4		
V_{GS}	Operating Range	Max	-1.8	-1.8	-1.8	-2.9	-2.9	-2.9	V	V_{DS}=10V I_D=30µA
I_GTYP.	Operating		-.25	-.25	-.25	-.500	-.500	-.500	pA	V_{DS}=10V I_D=30µA
I_GTYP.	High Temperature		-250	-250	-250	-500	-500	-500	pA	T_A=+125ºC
I_{GSS}TYP.	Gate Reverse Current		-1.0	-1.0	-1.0	-3.0	-3.0	-3.0	pA	V_{DS}=0V V_{GS}=-20V
I_{GSS}TYP.	Gate Reverse Current		1.0	1.0	1.0	3.0	3.0	3.0	nA	T_A=+125ºC

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-40	-60	--	V	V_{DS}= 0V I_G= -1nA
BV_{GGO}	Gate-to-Gate Breakdown	±40	--	--	V	I_{G1G2}= ±1µA I_D= 0A I_S= 0A
	TRANSCONDUCTANCE					
gfs	Full Conduction	300	--	1500	µS	V_{DS}= 10V V_{GS}= 0 f = 1kHz
gfs	Typical Operation	120	200	350	µS	V_{DG}= 10V I_D= 30µA f = 1kHz
	DRAIN CURRENT	60	--	1000	µA	U421-3 V_{DS}= 10V V_{GS}= 0
I_{DSS}	Full Conduction	60	--	1800	µA	U424-6

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	OUTPUT CONDUCTANCE					
g_{os}	Full Conduction	--	--	10	µS	V_{DS}= 10V V_{GS}= 0
g_{os}	Operating	--	0.1	3.0	µS	V_{DG}= 10V I_D= 30µA
	COMMON MODE REJECTION					
CMRR	-20 log $\lvert V_{GS1-2}/\Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 10 to 20V I_D=30µA
CMRR	-20 log $\lvert V_{GS1-2}/\Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 5 to 10V I_D=30µA
	NOISE					
NF	Figure	--	--	1.0	dB	V_{DG}= 10V, I_D= 30µA, R_G=10MΩ f= 10Hz
e_n	Voltage	--	20	70	nV/√Hz	V_{DG}= 10V I_D= 30µA f= 10Hz
			10			V_{DG}= 10V I_D= 30µA f= 1kHz
	CAPACITANCE					
C_{ISS}	Input	--	--	3.0	pF	V_{DS}= 10V V_{GS}= 0 f= 1MHz
C_{RSS}	Reverse Transfer	--	--	1.5	pF	V_{DS}= 10V V_{GS}= 0 f= 1MHz



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired
2. Derate 4mW/ºC above 25ºC
3. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicate electrical polarity only.

LINEAR SYSTEMS

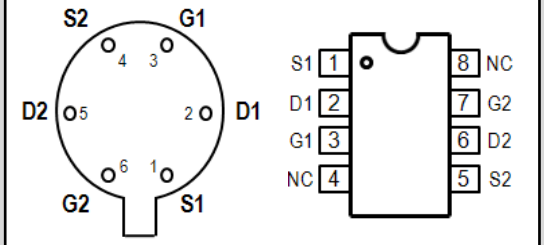
Improved Standard Products®

SST/U401 – SST/U406

LOW NOISE LOW DRIFT MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
LOW DRIFT	$\lvert V_{GS1-2}/T \rvert$ = 10µV/ºC TYP.
LOW NOISE	e_n=6nV/Hz@10Hz TYP.
LOW PINCHOFF	V_P=2.5V MAX.

ABSOLUTE MAXIMUM RATINGS NOTE 1 @ 25 °C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55 to +150°C
Operating Junction Temperature		-55 to +150°C
Maximum Voltage and Current for Each Transistor NOTE 1		
$-V_{GSS}$	Gate Voltage to Drain or Source	50V
$-V_{DSO}$	Drain to Source Voltage	50V
$-I_{G(f)}$	Gate Forward Current	10mA
Maximum Power Dissipation per side NOTE 2		
Device Dissipation TA = 25°C		300mW



TO-71 Top View

SOIC Top View

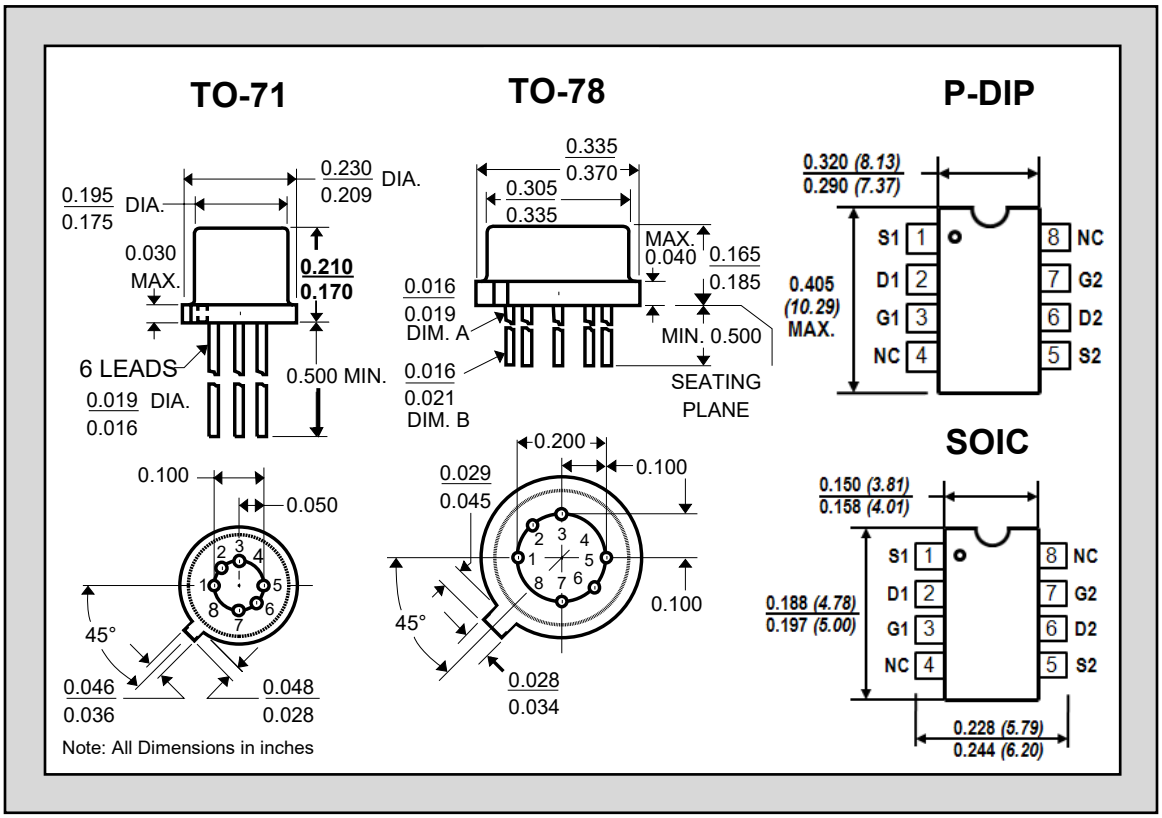
MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	U401	U402	U403	U404	U405	U406	UNITS	CONDITIONS
$\lvert V_{GS1-2}/T \rvert$ max.	Drift vs. Temperature	10	10	25	25	40	80	µV/ºC	V_{DG} = 10V, I_D = 200µA T_A = -55ºC to +125ºC
$\lvert V_{GS1-2} \rvert$ max.	Offset Voltage	5	10	10	15	20	40	mV	V_{DG} = 10V, I_D = 200µA

ELECTRICAL CHARACTERISTICS TA = 25ºC (unless otherwise noted) NOTE 3

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-50	-60	--	V	V_{DS}= 0 I_D= 1nA
BV_{G1G2}	Gate-to-Gate Breakdown	±50	--	--	V	I_G= ±1µA I_D= 0, I_S = 0
	TRANSCONDUCTANCE					
G_{fss}	Full Conduction	2000	--	7000	µS	V_{DG}= 10V V_{GS}= 0 f = 1kHz
G_{fs}	Typical Operation	1000	--	2000	µS	V_{DG}= 15V I_D= 200µA f = 1kHz
$\lvert G_{fs1}/G_{fs2} \rvert$	Mismatch	0.97	--	1.0		
I_{DSS}	Saturation Drain Current	0.5	--	10	mA	V_{DG}= 10V V_{GS}= 0
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Current Ratio	0.9	0.98	1.0		
	GATE VOLTAGE					
V_{GS}(off) or V_P	Pinchoff Voltage	-0.5	--	-2.5	V	V_{DS}= 15V I_D= 1nA
V_{GS}	Operating Range	--	--	-2.3	V	V_{DS}= 15V I_D= 200µA
	GATE CURRENT					
I_G	Operating	--	-4	-15	pA	V_{DG}= 15V I_D= 200µA
I_G	High Temperature	--	--	-10	nA	T_A=+125ºC
I_{GSS}	Gate Reverse Current	--	--	-100	pA	V_{GS}=-30v, V_{DS}= 0V
I_{G1G2}	Gate to Gate Isolation Current	--	--	±1.0	µA	V_{G1}-V_{G2}= ±50V, I_D= IS= 0

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	OUTPUT CONDUCTANCE					
G_{OSS}	Full Conduction	--	--	40	µS	V_{DS}= 10V, V_{GS}= 0V, f = 1kHz
G_{OS}	Operating	--	2	2.7	µS	V_{DS}= 15V, I_D= 200µA, f = 1kHz
	COMMON MODE REJECTION					V_{DG1}= 10V
CMRR	-20 log [(V_{GS1}-V_{GS2})/ΔV_{DG1-2}]	95	--	--	dB	V_{DG2}= 20V I_{D1}= I_{D2}=200µA
	NOISE					
NF	Figure	--	--	0.5	dB	V_{DS}= 15V V_{GS}= 0 R_G=10M f= 100Hz NBW= 6Hz
e_n	Voltage	--	6	20	nV/Hz	V_{DS}= 15V I_D= 200µA f= 10Hz NBW= 1Hz
	CAPACITANCE					
C_{ISS}	Input	--	4	8	pF	V_{DS}= 15V I_D= 200µA f= 1MHz
C_{RSS}	Reverse Transfer	--	1.5	3	pF	



Note: All Dimensions in inches

NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. Derate 2.4mW/ºC when TA is greater than 25ºC
3. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicate electrical polarity only.

LINEAR SYSTEMS

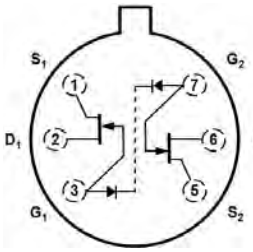
Improved Standard Products®

LS3954A LS3954 LS3955 LS3956 LS3958

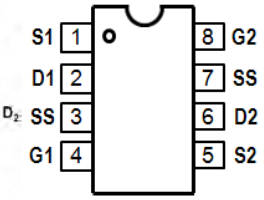
LOW NOISE LOW DRIFT MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
LOW DRIFT	$\lvert\Delta V_{GS1-2}/\Delta T\rvert$ =5µV/°C max.
LOW LEAKAGE	I_G=20pA TYP.
LOW NOISE	e_n=10Nv/√Hz TYP.

ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55 to +150°C
Operating Junction Temperature		-55 to +150°C
Maximum Voltage and Current for Each Transistor[1]		
$-V_{GSS}$	Gate Voltage to Drain or Source	60V
$-I_{G(f)}$	Gate Forward Current	50mV
Maximum Power Dissipation		
Device Dissipation @ Free Air - Total		400mW @ 25ºC[2]



Top View
TO-71 & TO-78



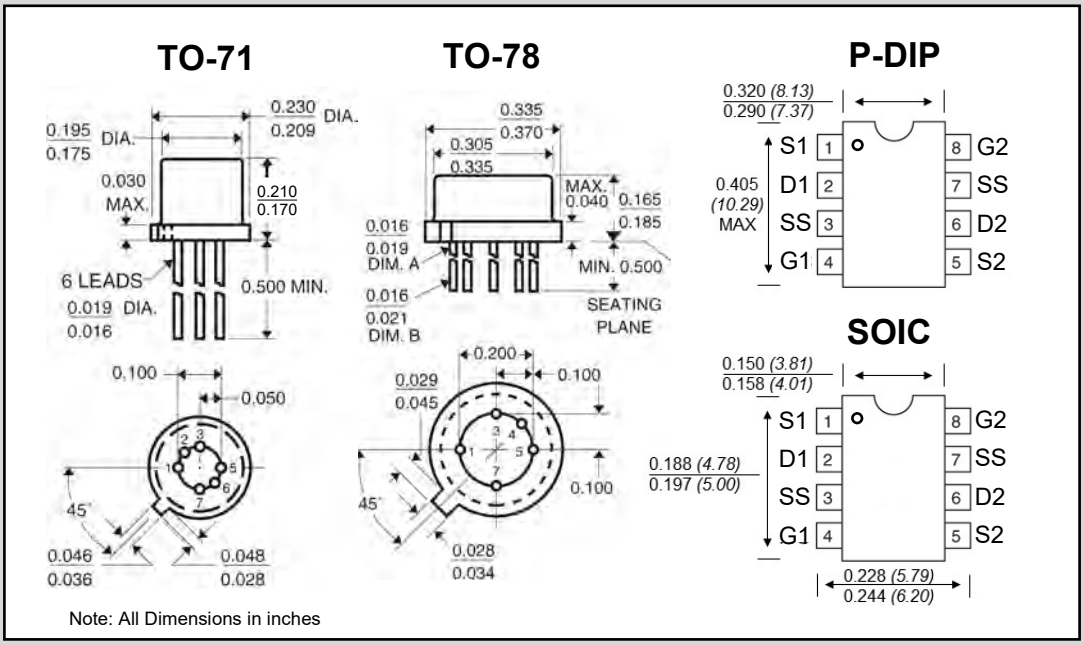
Top View
SOIC

ELECTRICAL CHARACTERISTICS @ 25ºC (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS3954A	LS3954	LS3955	LS3956	LS3958	UNITS	CONDITIONS
$\lvert\Delta V_{GS1-2}/\Delta T\rvert$ max.	Drift vs. Temperature	5	10	25	50	100	µV/ºC	V_{DG} = 20V, I_D=200µA T_A = -55ºC to +125ºC
$\lvert V_{GS1-2}\rvert$ max.	Offset Voltage	5	5	10	15	25	mV	V_{DG} =20V, I_D=200µA

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS		
BV_{GSS}	Breakdown Voltage	60	--	--	V	V_{DS}= 0	I_G= 1µA	
BV_{GGO}	Gate-to-Gate Breakdown	60	--	--	V	I_{GG}= ±1µA	I_D= 0	I_S= 0
	TRANSCONDUCTANCE							
g_{fss}	Full Conduction	1000	2000	4000	µS	V_{DG}= 20V	V_{GS}= 0	f = 1kHz
g_{fs}	Typical Operation	500	700	1250	µS	V_{DG}= 20V	I_D= 200µA	
$\lvert g_{fs1-2}/g_{fs}\rvert$	Differential	--	±0.6	±3	%			
	DRAIN CURRENT							
I_{DSS}	Full Conduction	0.5	2	5	mA	V_{DS}= 20V	V_{GS}= 0	
$\lvert I_{DSS1-2}/I_{DSS}\rvert$	Differential	--	±1	±5	%			
	GATE VOLTAGE							
V_{GS}(off)	Pinchoff Voltage	-1	-2	-4.5	V	V_{DS}= 20V	I_D= 1nA	
V_{GS}	Operating Range	-0.5	--	-4	V	V_{DS}= 20V	I_D= 200µA	
	GATE CURRENT							
$-I_G$	Operating	--	20	50	pA	V_{DG}= 20V	I_D= 200µA	
$-I_G$	High Temperature	--	--	50	nA	V_{DG}= 20V	I_D= 200µA	T_A=+125 ºC
$-I_G$	Reduced V_{DG}	--	5	--	pA	V_{DG}= 10V	I_D= 200µA	
$-I_{GSS}$	At Full Conduction	--	--	100	pA	V_{DG}= 20V	V_{DS}= 0	

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	OUTPUT CONDUCTANCE					
g_{oss}	Full Conduction	--	--	35	µS	V_{DG}= 20V V_{GS}= 0
g_{os}	Operating	--	0.5	1	µS	V_{DG}= 20V I_D= 200µA
$\lvert g_{os1-2} \rvert$	Differential	--	0.05		µS	
	COMMON MODE REJECTION					
CMRR	-20 log $\lvert \Delta V_{GS1-2}/\Delta V_{DS} \rvert$	--	100	--	dB	ΔV_{DS}= 10 to 20V I_D=200µA
CMRR	-20 log $\lvert \Delta V_{GS1-2}/\Delta V_{DS} \rvert$	--	75	--	dB	ΔV_{DS}= 5 to 10V I_D=200µA
	NOISE					
NF	Figure	--	--	0.5	dB	V_{DS}= 20V V_{GS}= 0 R_G=10MΩ f= 100Hz NBW=6Hz
e_n	Voltage	--	--	15	nV/√Hz	V_{DS}= 20V I_D= 200µA f= 10Hz NBW=1Hz
	CAPACITANCE					
C_{ISS}	Input	--	--	6	pF	V_{DS}= 20V V_{GS}= 0 f= 1MHz
C_{RSS}	Reverse Transfer	--	--	2	pF	
C_{DD}	Drain-to-Drain	--	0.1	--	pF	V_{DG}= 20V I_D= 200µA



Note: All Dimensions in inches

NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. Derate 4mWºC above 25ºC

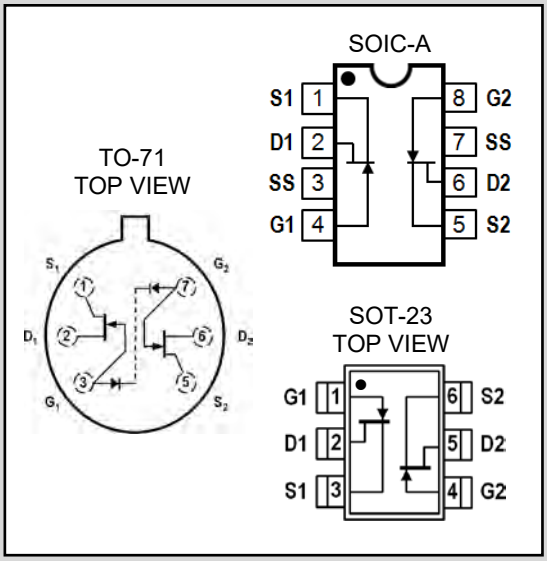
LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

LSK589

LOW NOISE, LOW CAPACITANCE MONOLITHIC DUAL N-CHANNEL JFET

FEATURES	
ULTRA LOW NOISE	e_n = 4.0 nV/√Hz
LOW INPUT CAPACITANCE	Ciss = 5pF
HIGH TRANSCONDUCTANCE	Gfs ≥ 4000µS



ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation, TA = 25°C	
Continuous Power Dissipation, per side [4]	250mW
Power Dissipation, total [5]	500mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 50mA
Maximum Voltages	
Gate to Source	V_{GSO} = 25V
Gate to Drain	V_{GDO} = 25V

MATCHING CHARACTERISTICS @ 25°C (unless otherwise stated)

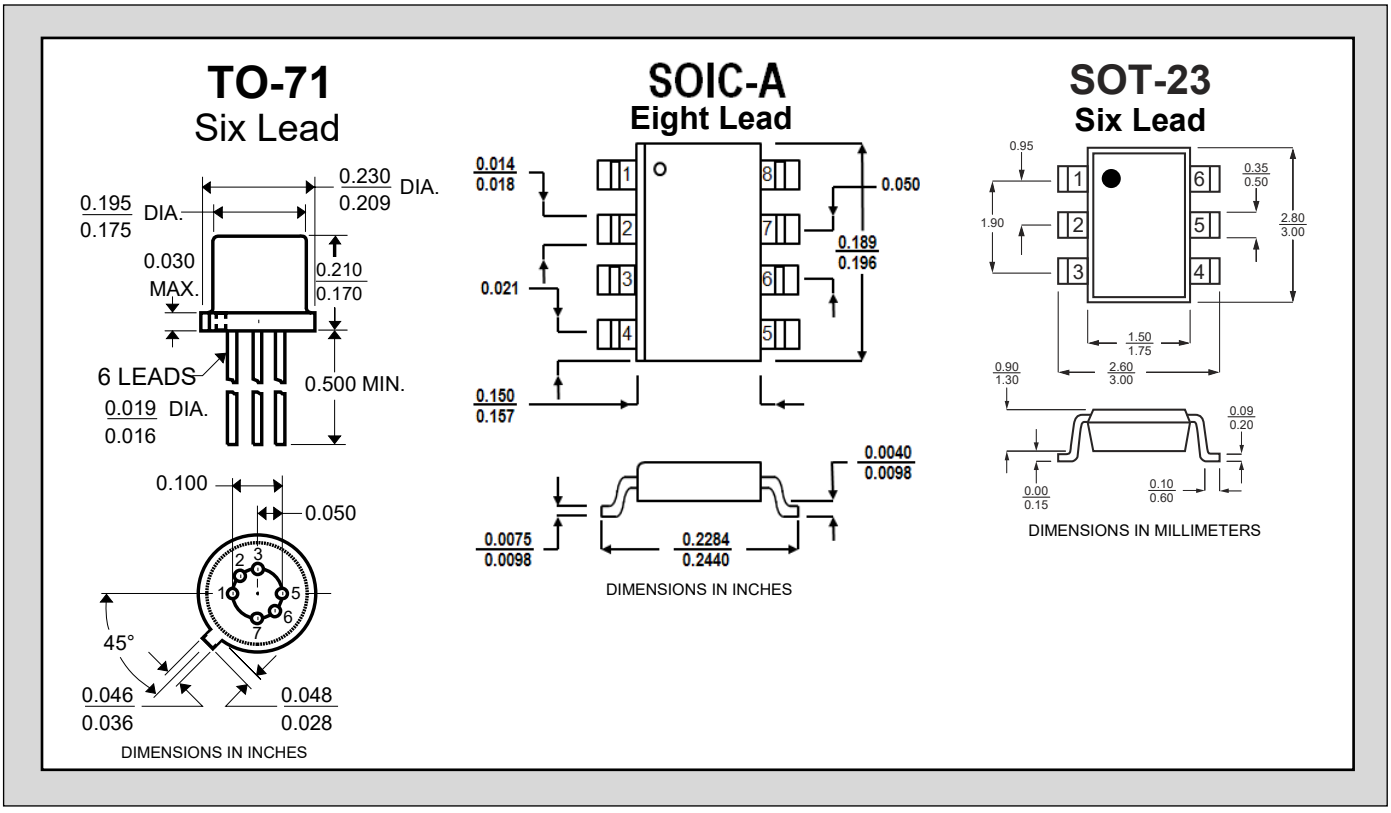
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate to Source Cutoff Voltage			20	mV	V_{DS} = 10V, I_D = 5mA
$\frac{I_{DSS1}}{I_{DSS2}}$	Gate to Source Saturation Current Ratio	0.9		1.0		V_{DS} = 10V, V_{GS} = 0V (Note 2)
CMRR	**COMMON MODE REJECTION RATIO** $-20 \log \lvert \Delta V_{GS1-2}/\Delta V_{DS} \rvert$	85			dB	V_{DG} = 5V to 10V, I_D = 5mA

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
e_n	Noise Voltage		7		nV/√Hz	V_{DS} = 10V, I_D = 5mA, *f* = 100Hz
e_n	Noise Voltage		4		nV/√Hz	V_{DS} = 10V, I_D = 5mA, *f* = 10kHz
C_{ISS}	Common Source Input Capacitance			5	pF	V_{DS} = 10V, I_D = 5mA, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Capacitance			1.2	pF	

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage		-25			V	V_{DS} = 0, I_D = 1µA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage		-1.5		-5	V	V_{DS} = 10V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage		-0.3		-4.0	V	V_{DS} = 10V, I_D = 5mA
I_{DSS}	Drain to Source Saturation Current		7.0		40	mA	V_{DS} = 10V, V_{GS} = 0V (Note 2)
I_G	Gate Operating Current			-1	-50	pA	V_{DG} = 10V, I_D = 5mA
I_{GSS}	Gate to Source Leakage Current				-50	pA	V_{gs} = -15V, V_{DS} = 0
G_{OS}	Output Conductance F = 1kHz				100	µS	V_{DS} = 10V, I_D = 5mA
NF	Noise Figure				1.0	dB	V_{DS} = 10V, I_D = 5mA, R_G = 100KΩ, *f* = 100Hz
G_{fs}	Forward Transconductance	*f* = 1kHz	4000		10000	µS	V_{Ds} = 10V, I_D = 5mA
		f = 100MHz		7000			
Gos	Output Transconductance	*f* = 1kHz			100		
		f = 100MHz		120			

PACKAGE DIMENSIONS



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300 µs, Duty Cycle ≤ 3%
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate electrical polarity only.
4. Derate 2.0 mW/°C above 25°C.
5. Derate 4 mW/°C above 25°C.

LINEAR SYSTEMS

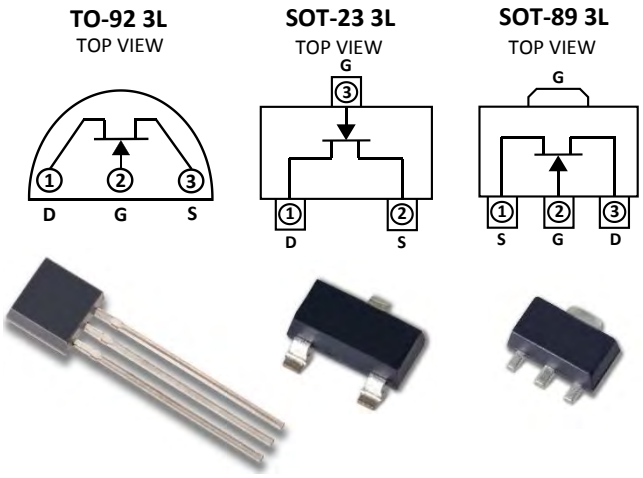
Over 30 Years of Quality Through Innovation

LSK170 A/B/C/D

High Input Impedance, Ultra-Low Noise, Single N-Channel JFET

Ultra-Low Noise at Both High & Low Frequencies With a Narrow Range of IDSS

Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +135°C
Maximum Power Dissipation	
Continuous Power Dissipation @ +25°C	400mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = 40V
Gate to Drain	V_{GDS} = 40V



Features

- ULTRA LOW NOISE (*f* =1khz): e_n = 0.9nV/√Hz
- High Breakdown Voltage: BV_{GSS} = 40V min
- High Gain: G_{fs} = 22mS (typ)
- High Input Impedance: 20GΩ typ
- Low Capacitance: 22pF max
- Improved Second Source Replacement for 2SK170
- For Equivalent Monolithic-Dual, See the LSK389 Series

Benefits

- Direct Pin-For-Pin Replacement of Toshiba's 2SK170
- Optimized to Provide Low Noise at Both High and Low Frequencies With a Narrow Range of IDSS and Low Capacitance
- Low Noise to Capacitance Ratio and Narrow Range of Low Value IDSS Provide Solutions for Low Noise Applications Which Cannot Tolerate High Values of Capacitance or Wide Ranges of IDSS

Applications

- Audio Amplifiers and Preamps
- Discrete Low-Noise Operational Amplifiers
- Guitar Pickups
- Effects Pedals
- Microphones
- Audio Mixer Consoles
- Acoustic Sensors
- Sonobouys
- Hydrophones

Applications Cont'd

- Chemical and Radiation Detectors
- Instrumentation Amplifiers
- Accelerometers
- CT Scanners Input Stages
- Oscilloscope Input Stages
- Electrometers and Vibrations Detectors

Description

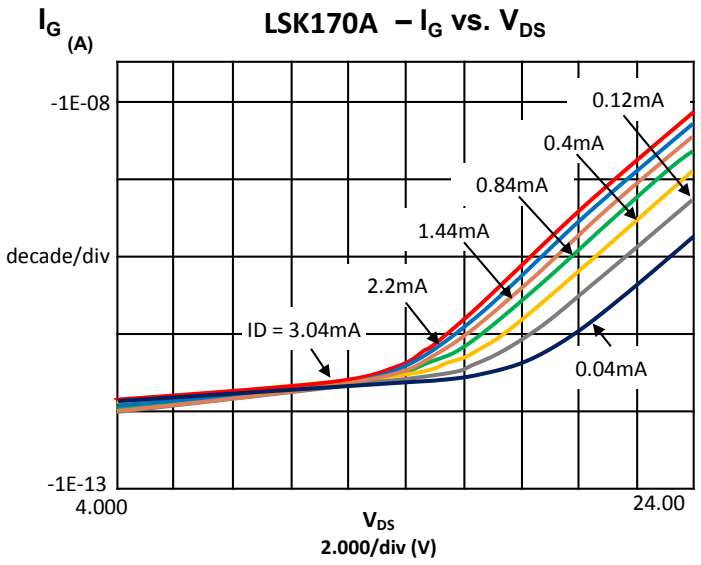
The LSK170 is specifically designed for low noise, high input impedance applications within the audio, instrumentation, medical and sensors markets. The narrow ranges of I_{DSS} grades with the LSK170 promote ease of design, particularly in low voltage applications. The LSK170 is ideal for portable battery operated applications, and features high BV_{DSS} for maximum linear headroom in high transient program content amplifiers. The series has a uniquely linear V_{GS} transfer function for a stability that is highly desirable, particularly for audio front-end preamplifiers. The device is available in a surface mount SOT-23 package, through-hole TO-92 package and SOT-89 package. The surface mount version of the LSK170 Series creates new opportunities for engineers seeking to design lower noise circuits in compact embeddable applications where shielding and space are critical. The LSK170 series is a pin for pin replacement of the Toshiba 2SK170 and improved functional replacement for the Interfet IF1320, IF1330, IF1331, and IF4500. Contact the factory for tighter noise and other specification selections.

Electrical Characteristics @ 25°C (unless otherwise stated)

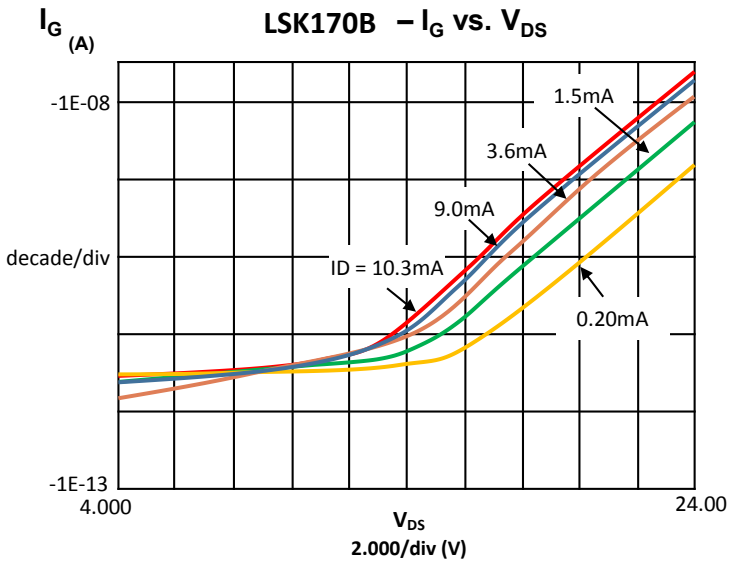
SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage		-40.0			V	V_{DS} = 0V, I_D = -100µA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage		-0.2		-2.0	V	V_{DS} = 10V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage			0.5		V	V_{DS} = 10V, I_D = 1mA
I_{DSS}[2]	Drain to Source Saturation Current	LSK170A	2.6		6.5	mA	V_{DS} = 10V, V_{GS} = 0
		LSK170B	6.0		12.0		
		LSK170C	10.0		20.0		
		LSK170D	18.0		30.0		
I_G	Gate Operating Current				-0.5	nA	V_{DG} = 10V, I_D = 1mA
I_{GSS}	Gate to Source Leakage Current				-1.0	nA	V_{Gs} = -10V, V_{Ds} = 0V
G_{fs}	Full Conduction Transconductance		14.0	22.0		mS	V_{DS} = 10V, V_{GS} = 0, *f* = 1kHz
G_{fs}	Typical Conduction Transconductance		6.0	10.0		mS	V_{DS} = 15V, I_D = 1mA
e_n	Noise Voltage			0.9	1.9	nV/√Hz	V_{DS} = 10V, I_D = 2mA, *f* = 1kHz, NBW = 1Hz
e_n	Noise Voltage			1.4	4.0	nV/√Hz	V_{DS} = 10V, I_D = 2mA, *f* = 10Hz, NBW = 1Hz
C_{ISS}	Common Source Input Capacitance			20.0		pF	V_{DS} = 15V, I_D = 100µA, *f* = 1MHz,
C_{RSS}	Common Source Reverse Transfer Cap.			5.0		pF	V_{DS} = 15V, I_D = 100µA, *f* = 1MHz,

Typical Characteristics

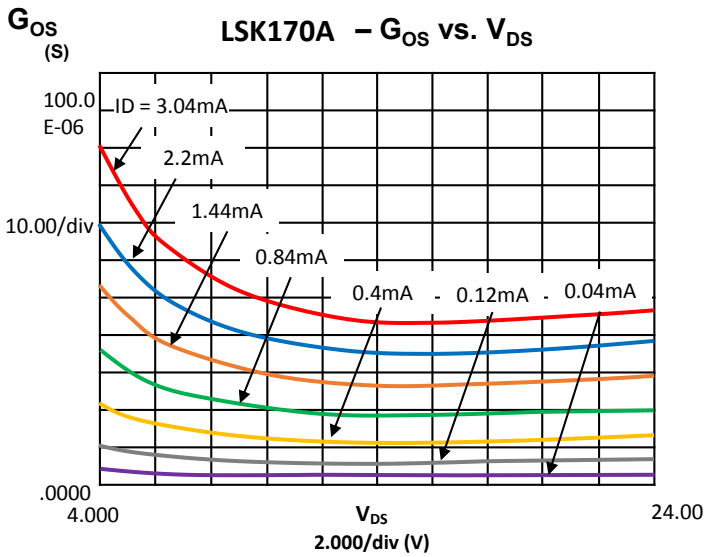
Operating Current



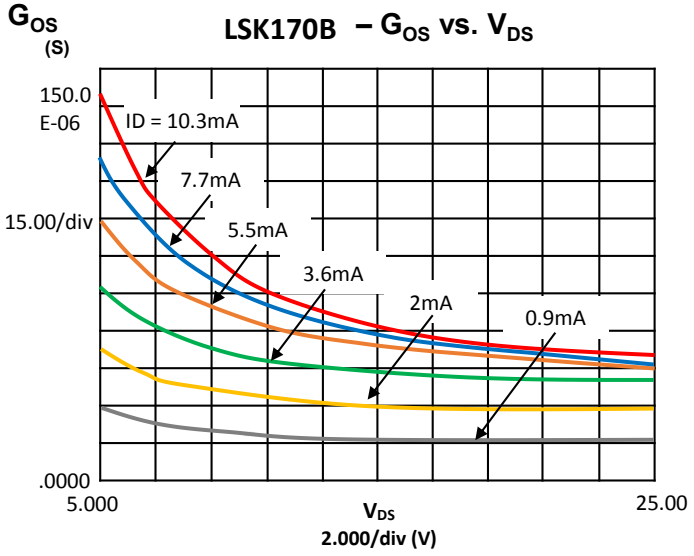
Operating Current



Output Conductance

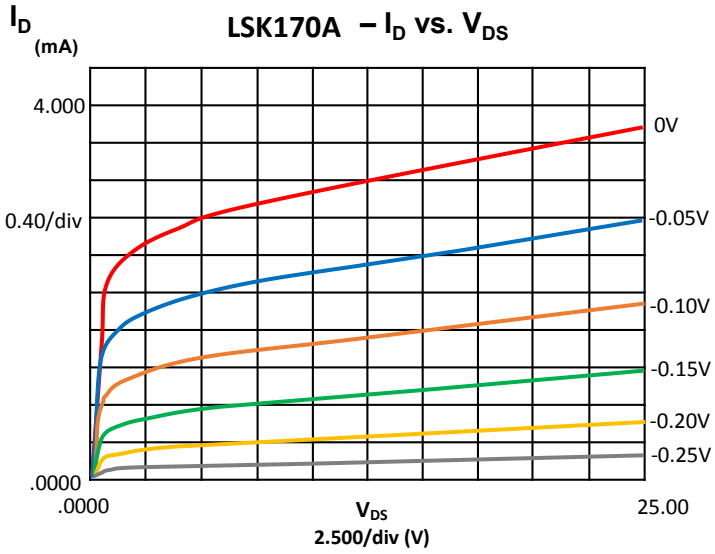


Output Conductance

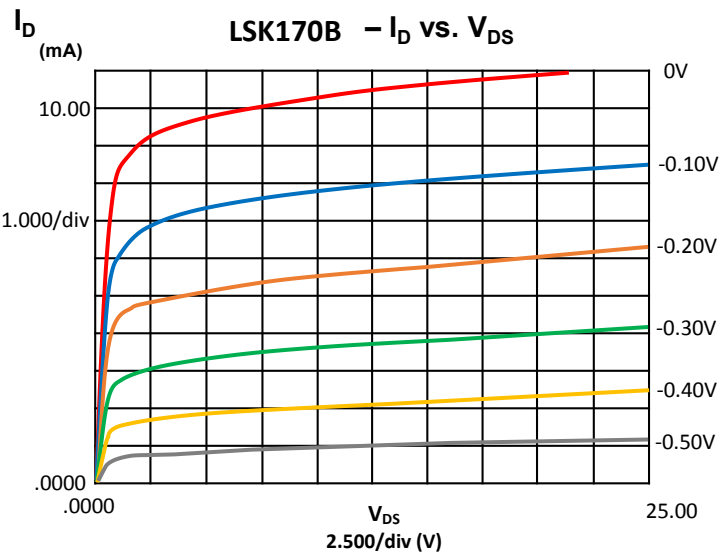


Typical Characteristics Continued

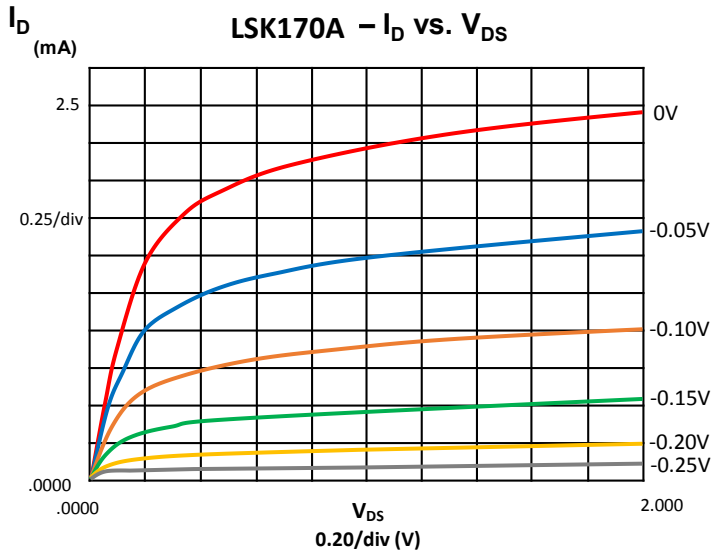
Output Characteristics



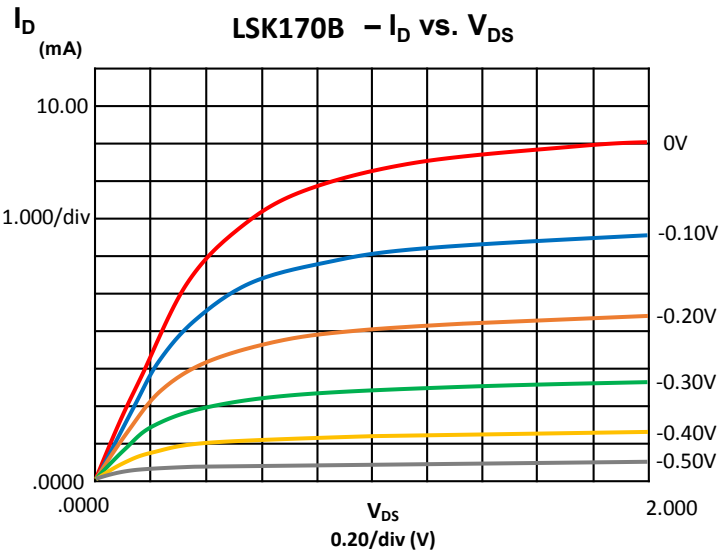
Output Characteristics



Operating Characteristics

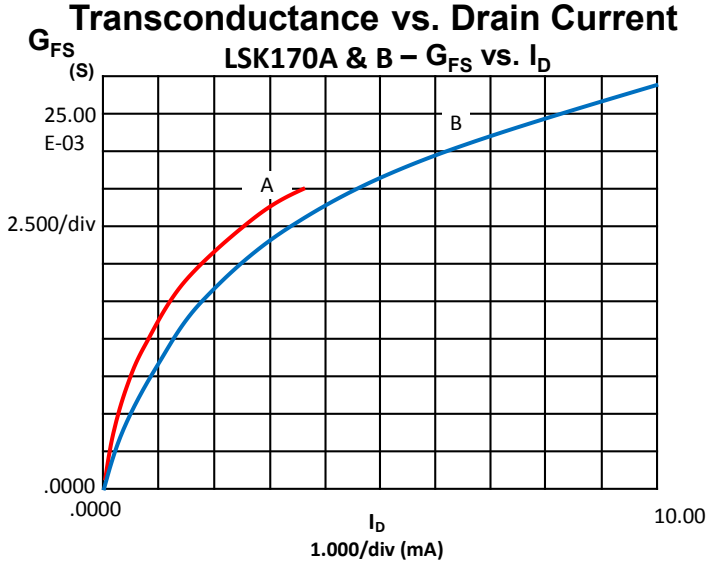


Operating Characteristics

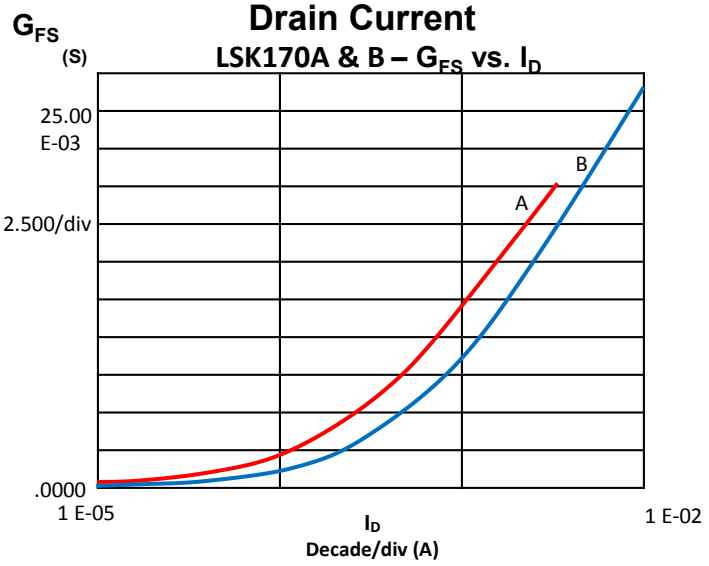


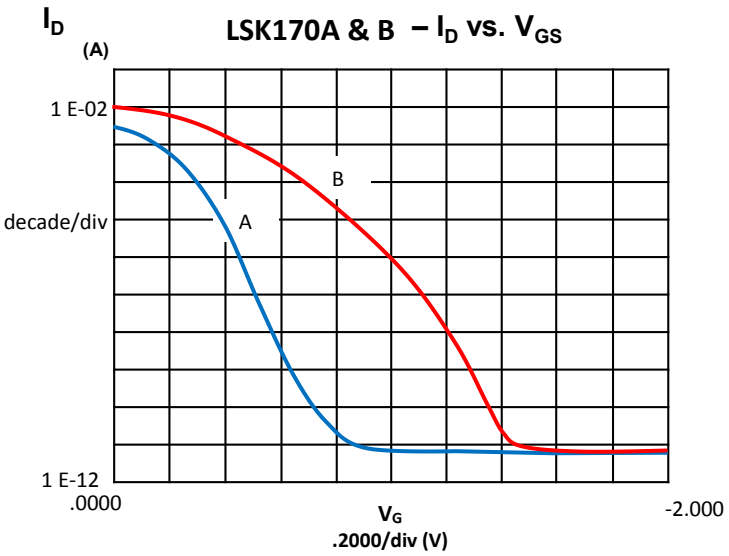
Typical Characteristics Continued

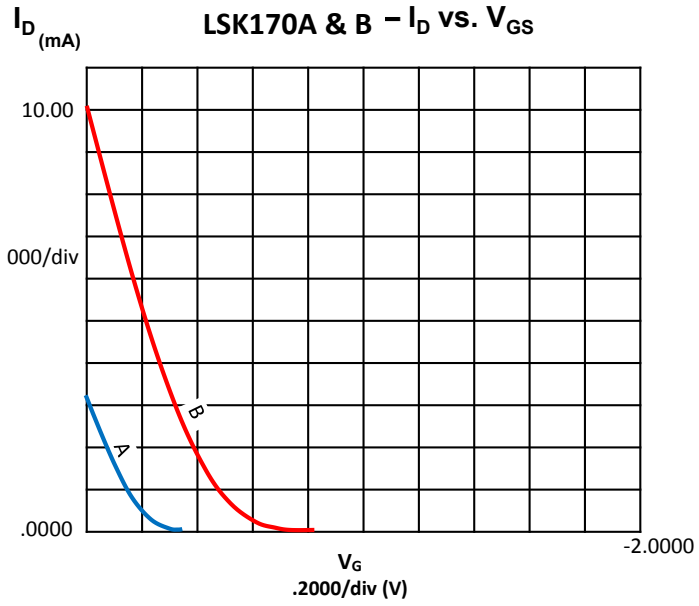
Common Source Forward Transconductance vs. Drain Current



Common Source Transconductance vs. Drain Current

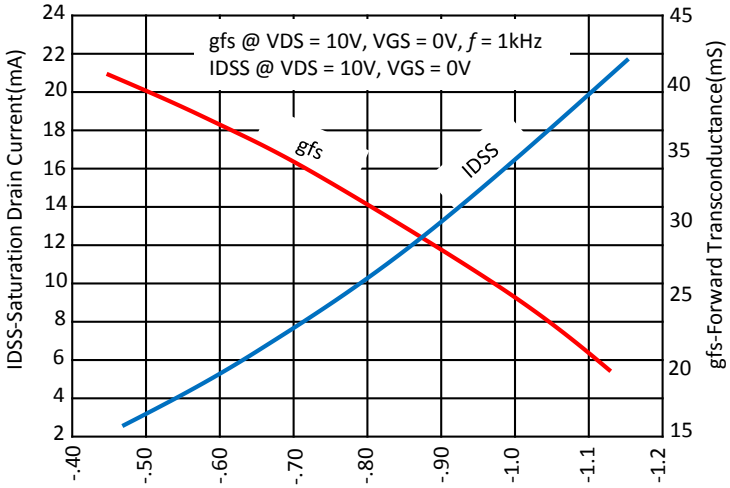




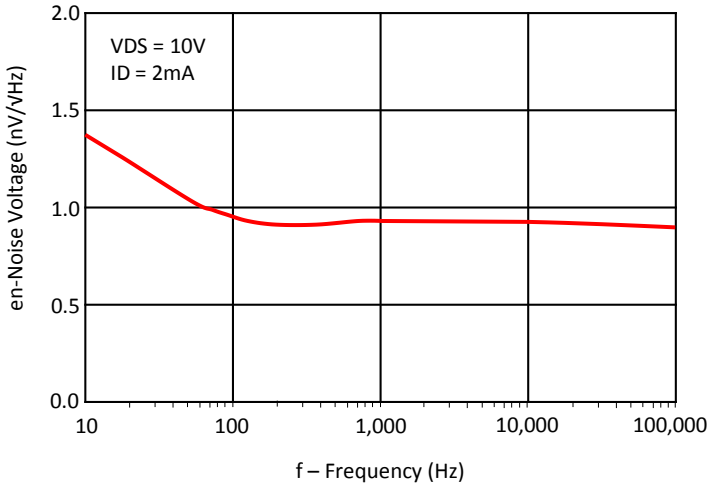


Typical Characteristics Continued

Drain Current Transconductance vs. Gate-Source Cutoff Voltage



Equivalent Input Noise Voltage vs. Frequency

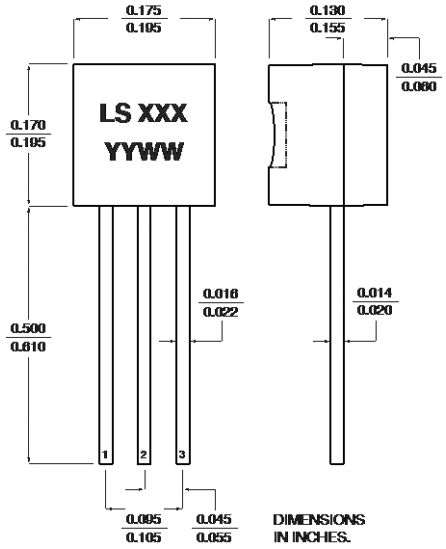


Ordering Information

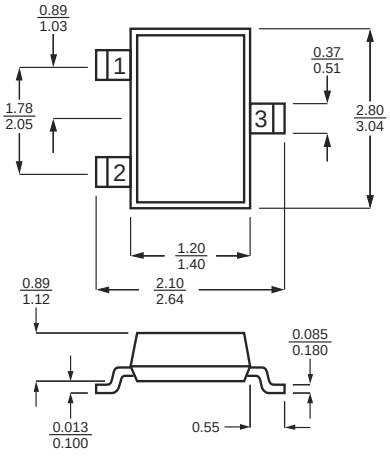
STANDARD PART CALL-OUT	CUSTOM PART CALL-OUT CUSTOM PARTS INCLUDE SEL + 4 DIGIT NUMERIC CODE)
LSK170A TO-92 3L RoHS	LSK170A TO-92 3L RoHS SELXXXX
LSK170B TO-92 3L RoHS	LSK170B TO-92 3L RoHS SELXXXX
LSK170C TO-92 3L RoHS	LSK170C TO-92 3L RoHS SELXXXX
LSK170D TO-92 3L RoHS	LSK170D TO-92 3L RoHS SELXXXX
LSK170A SOT-23 3L RoHS	LSK170A SOT-23 3L RoHS SELXXXX
LSK170B SOT-23 3L RoHS	LSK170B SOT-23 3L RoHS SELXXXX
LSK170C SOT-23 3L RoHS	LSK170C SOT-23 3L RoHS SELXXXX
LSK170D SOT-23 3L RoHS	LSK170D SOT-23 3L RoHS SELXXXX
LSK170A SOT-89 3L RoHS	LSK170A SOT-89 3L RoHS SELXXXX
LSK170B SOT-89 3L RoHS	LSK170B SOT-89 3L RoHS SELXXXX
LSK170C SOT-89 3L RoHS	LSK170C SOT-89 3L RoHS SELXXXX
LSK170D SOT-89 3L RoHS	LSK170D SOT-89 3L RoHS SELXXXX

Package Dimensions

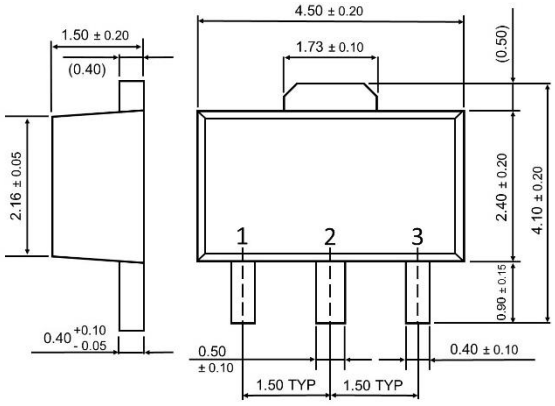
TO-92 3 Lead



SOT-23 3 Lead



SOT-89 3 Lead



Notes:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.
4. When ordering include the full Linear Systems part number and package type. Linear Systems creates custom parts on a case by case basis. To learn whether Linear Systems can meet your requirements, please send your drawing along with a detailed description of the device specifications to sales@linearsystems.com. One of our qualified representatives will contact you.
5. All standard parts are RoHS compliant. Contact the factory for availability of non-RoHS parts.
6. Information furnished by Linear Integrated Systems is believed to be accurate and reliable. However, no responsibility is assumed for its use; nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Linear Integrated Systems.
7. Voltage specifications are not tested 100%, but guaranteed by lot sampling. Contact the factory if 100% test is required.

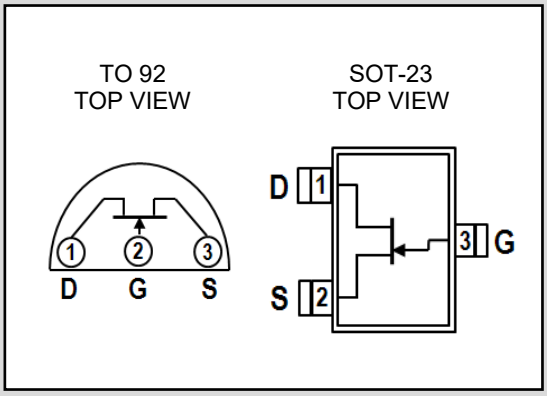
LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

LSK189

LOW NOISE, LOW CAPACITANCE SINGLE N-CHANNEL JFET

FEATURES	
ULTRA LOW NOISE	e_n = 1.8nV/√Hz
LOW INPUT CAPACITANCE	C_{ISS} = 4pF
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation TA=25°C	300mW[4]
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSO} = 60V
Gate to Drain	V_{GDO} = 60V

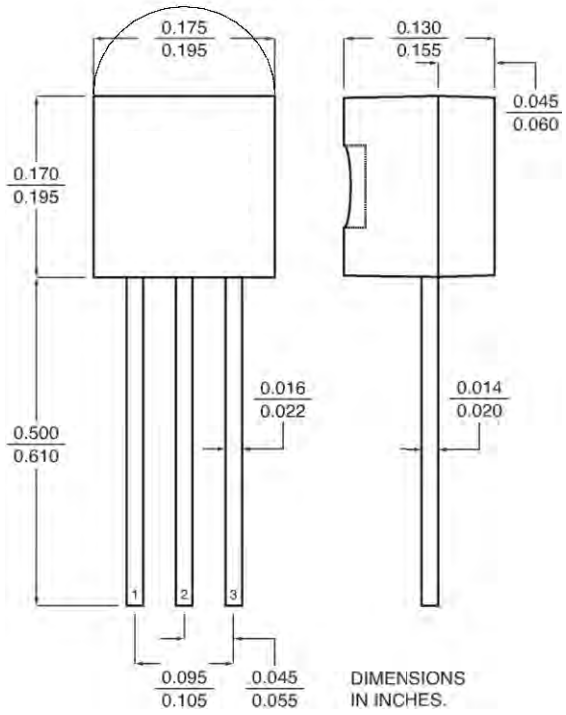


* For equivalent monolithic dual, see LSK489

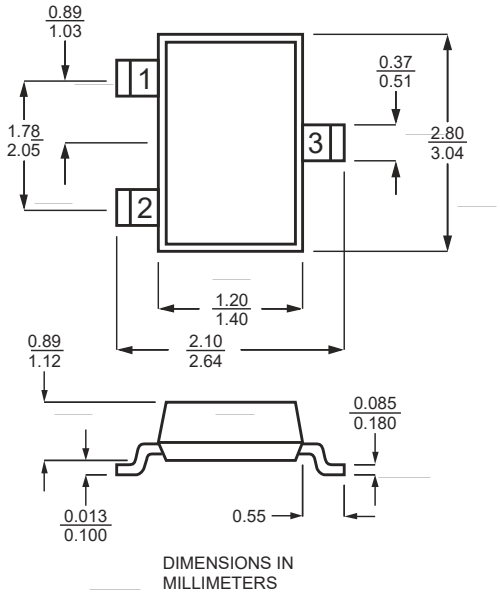
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-60			V	V_{DS} = 0, I_D = -1nA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-1.5		-3.5	V	V_{DS} = 15V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage	-0.5		-3.5	V	V_{DS} = 15V, I_D = 500µA
I_{DSS}[2]	Drain to Source Saturation Current	2.5	5	15	mA	V_{DS} = 15V, V_{GS} = 0
I_G	Gate Operating Current		-2	-25	pA	V_{DG} = 15V, I_D = 200µA
I_G			-0.8	-10	nA	TA=125°C
I_{GSS}	Gate to Source Leakage Current			-100	pA	V_{GS} = -15V
G_{fs}	Full Conductance Transconductance	1500			µS	V_{DS} = 15V, V_{GS} = 0, *f* = 1kHz
		1000	1500		µS	V_{DS} = 15V, I_D = 500µA
G_{OS}	Full Output Conductance			40	µS	V_{DS} = 15V, V_{GS} = 0
G_{OS}	Output Conductance		1.8	2.7	µS	V_{DS} = 15V, I_D = 200µA
NF	Noise Figure			0.5	dB	V_{DS} = 15V, V_{GS} = 0, R_G = 10MΩ, *f* = 100Hz, NBW = 6Hz
e_n	Noise Voltage		1.8	2.0	nV/√Hz	V_{DS} = 15V, I_D = 2mA, *f* = 1kHz, NBW = 1Hz
e_n	Noise Voltage		2.8	3.5	nV/√Hz	V_{DS} = 15V, I_D = 2mA, *f* = 10Hz, NBW = 1Hz
C_{ISS}	Common Source Input Capacitance		4	8	pF	V_{DS} = 15V, I_D = 500µA, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Cap.			3	pF	

Standard Package Dimensions:

TO-92



SOT-23

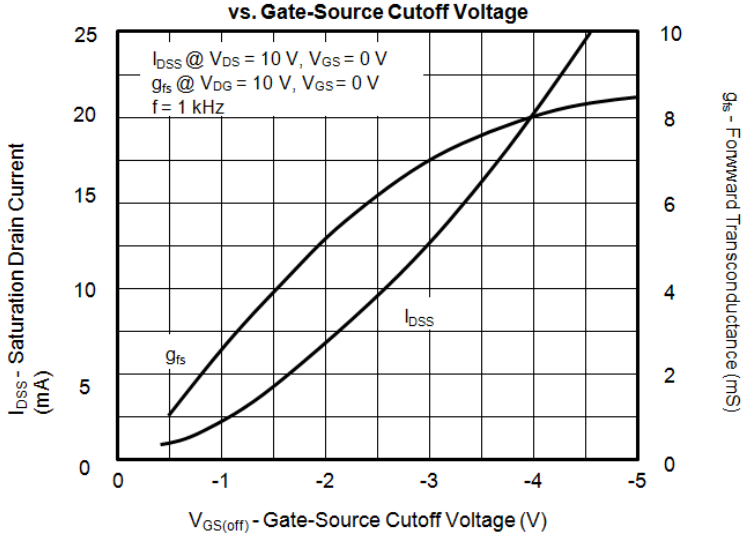


NOTES:

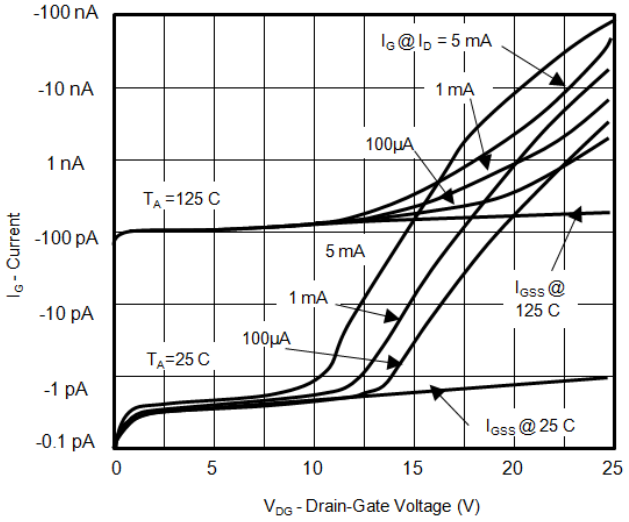
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300μs, Duty Cycle ≤ 3%.
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.
4. Derate 2.8 mW °C above 25°C.

LSK189 Typical Characteristics

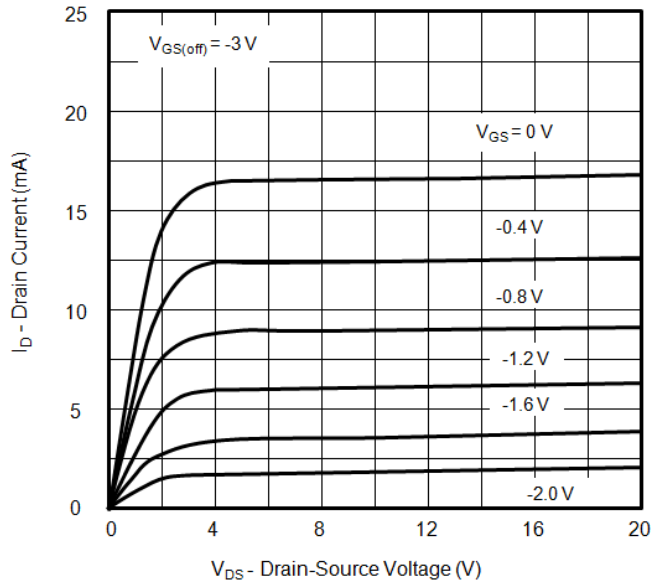
Drain Current and Transconductance vs. Gate-Source Cutoff Voltage



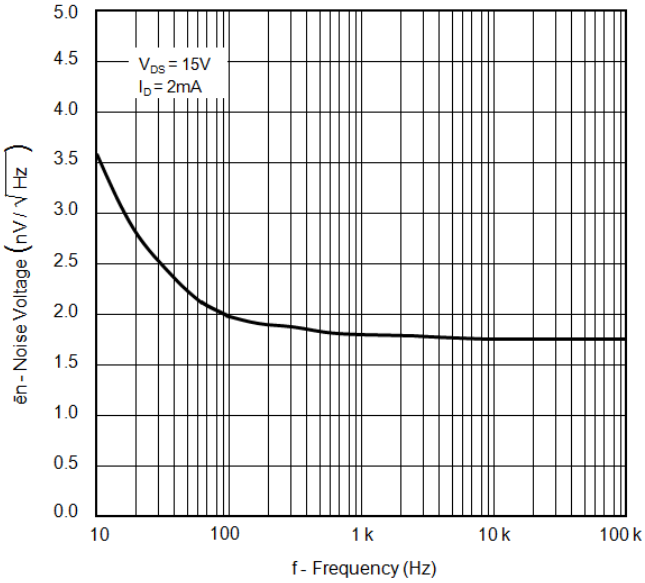
Operating Gate Current



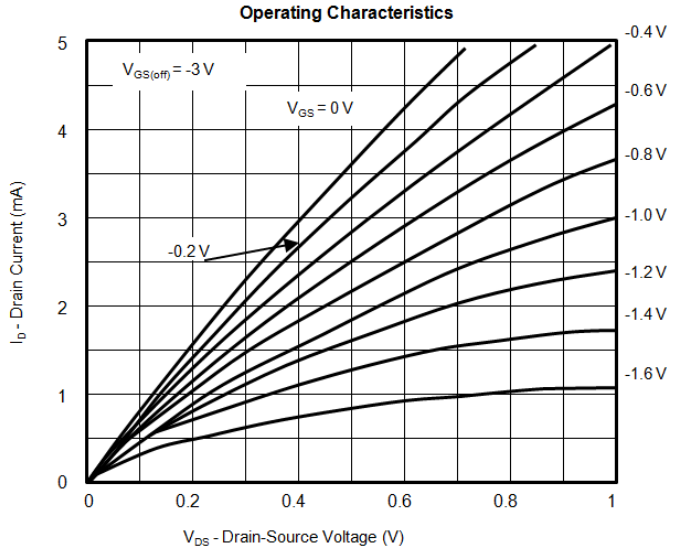
Output Characteristics



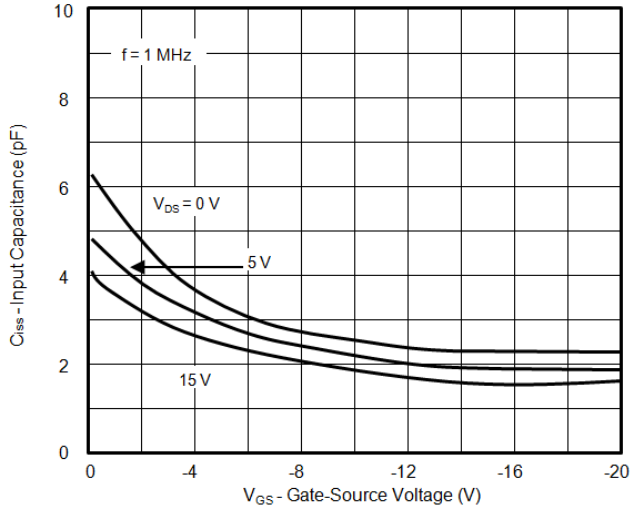
Equivalent Input Noise Voltage vs. Frequency



Operating Characteristics

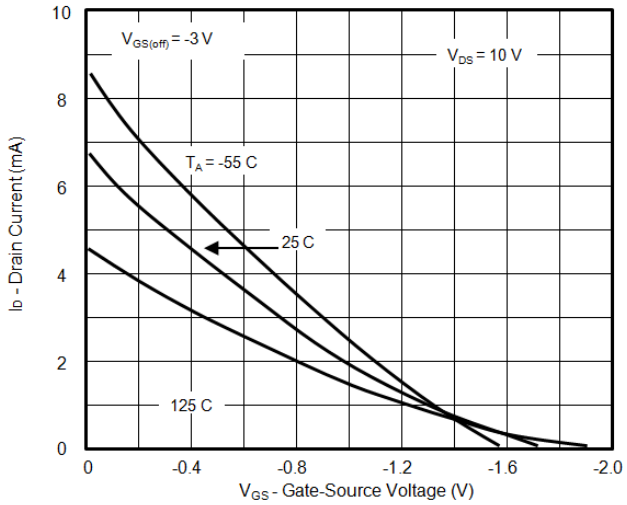


Common-Source Input Capacitance vs. Gate-Source Voltage

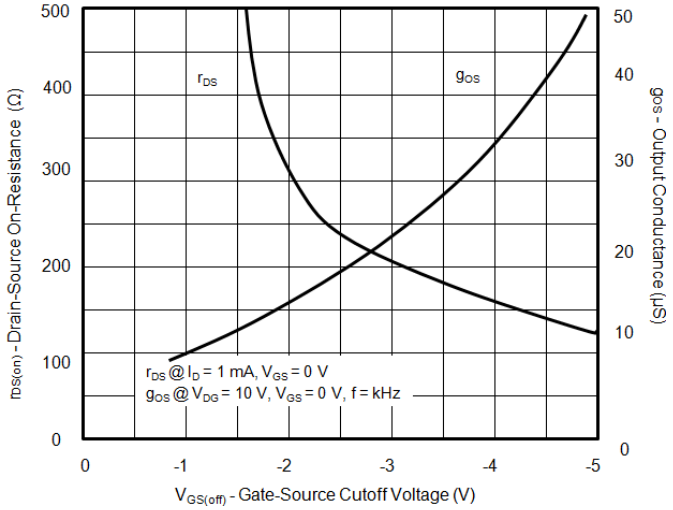


LSK189 Typical Characteristics Continued

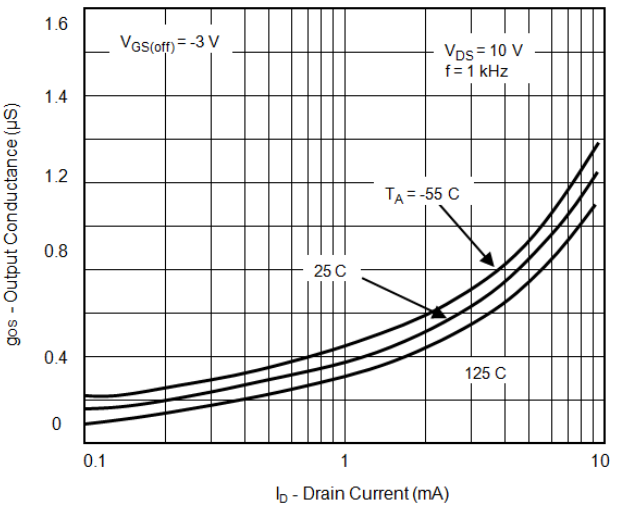
Transfer Characteristics



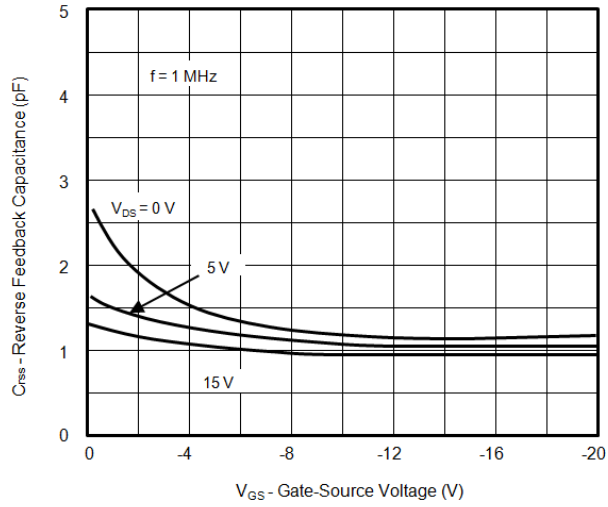
On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage



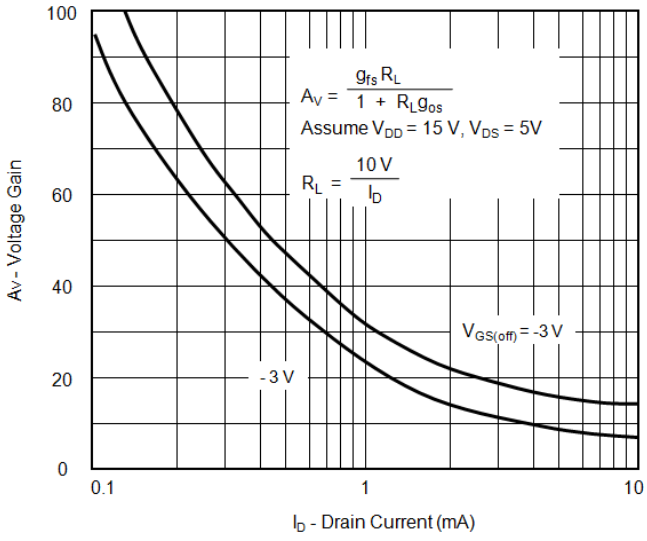
Output Conductance vs. Drain Current



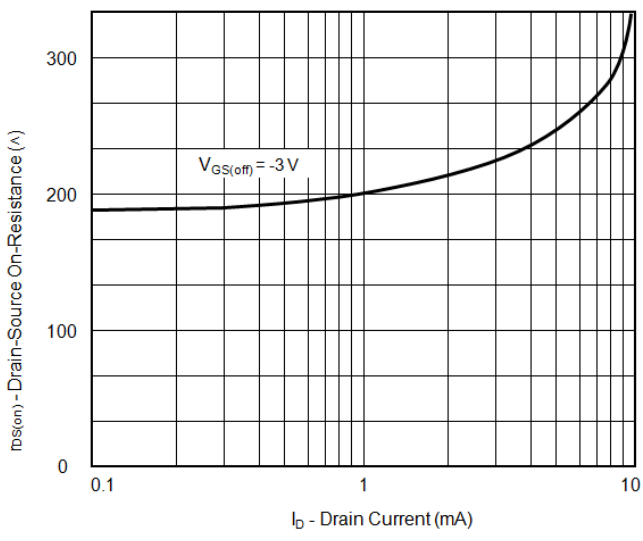
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



Circuit Voltage Gain vs. Drain Current

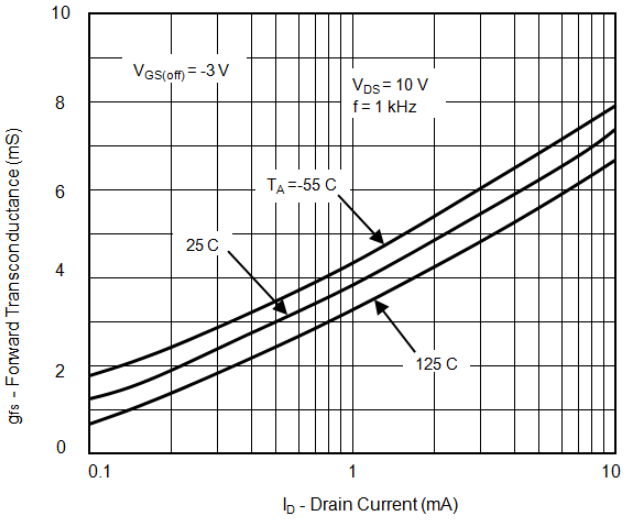


On-Resistance vs. Drain Current



LSK189 Typical Characteristics Continued

Common-Source Forward Transconductance vs. Drain Current



LINEAR SYSTEMS

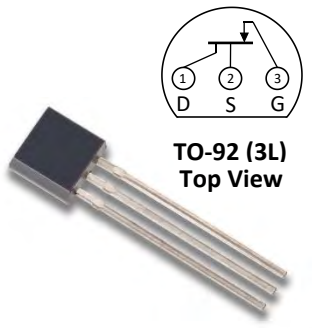
Improved Standard Products®

J/SST201/2/4

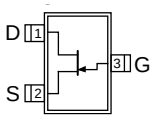
High Gain, Single N-Channel JFET Amplifier

General Purpose, Low Noise, Low Cost, Single JFET

Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation @ +25°C	350mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = 40V
Gate to Drain	V_{GDS} = 40V



TO-92 (3L)
Top View



SOT-23 (3L)
Top View

Features

- Low Cutoff Voltage: J201 <1.5V
- High Input Impedance
- Very Low Noise
- High Gain: AV = 80 @ 20 µA
- Reverse Gate to Source and Drain Voltage ≥| -40V

Benefits

- Low Cost
- Excellent Low Power Supply Operation
- Power Supply: Down to 1.5V
- Low Signal Loss/System Error
- High System Sensitivity
- High Quality Low-Level Signal

Applications

- High-Gain, Low Noise Amplifiers
- Low-Current, Low-Voltage Battery-Powered Amplifiers
- Infrared Detector Amplifiers
- Ultra-High Input Impedance Pre-Amplifiers

Description

The J/SST201/2/4 series is a low cost direct replacement for Siliconix J/SST201/2/4 series. Features include low leakage, very low noise, low cutoff voltage ($V_{GS(off)}$ ≤ 1.5V) and high Gain (A_V = 80 V/V) for use with low-level power supplies. The J/SST201/2/4 is excellent for battery powered equipment and low current amplifiers. The J series, TO-226 (TO-92) plastic package, provides low cost, while the SST series, TO-236 (SOT-23) package provides surface-mount capability. Both the J and SST series are available in tape-and-reel for automated assembly and in die form for automated assembly.

Electrical Characteristics @ 25 °C (unless otherwise stated)

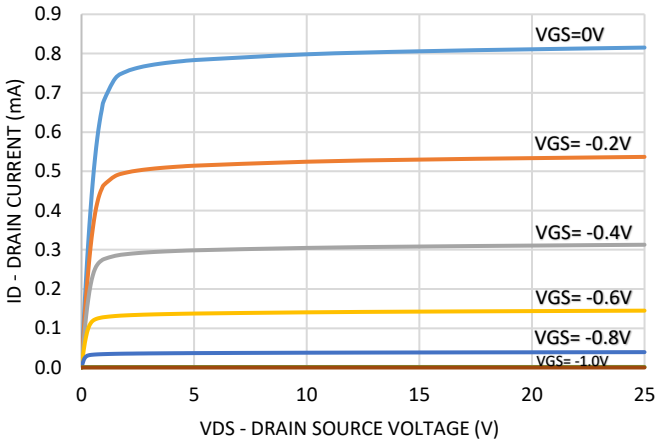
SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	J/SST201, 202	-40			V	I_G = -1µA, V_{DS} = 0.0V
		J/SST204	-25				
$V_{GS(off)}$	Gate to Source Cutoff Voltage	J/SST201	-0.3		-1.5		V_{DS} = 15V, I_D = 10nA
		J/SST202	-0.8		-4.0		
		J/SST204	-0.2		2.0		
I_{DSS}	Drain to Source Saturation Current[2]	J/SST201	0.2		1.0	mA	V_{DS} = 15V, V_{GS} = 0.0V
		J/SST202	0.9		4.5		
		J/SST204	0.2		3.0		
I_{GSS}	Gate Reverse Current				-100	pA	V_{GS} = -20V, V_{DS} = 0.0V
I_G	Gate Operating Current			-2			V_{DG} = 10V, I_D = 0.1mA
$I_{D(off)}$	Drain Cutoff Current			2			V_{DS} = 15V, V_{GS} = 5.0V

Electrical Characteristics @ 25 °C (unless otherwise stated) Continued

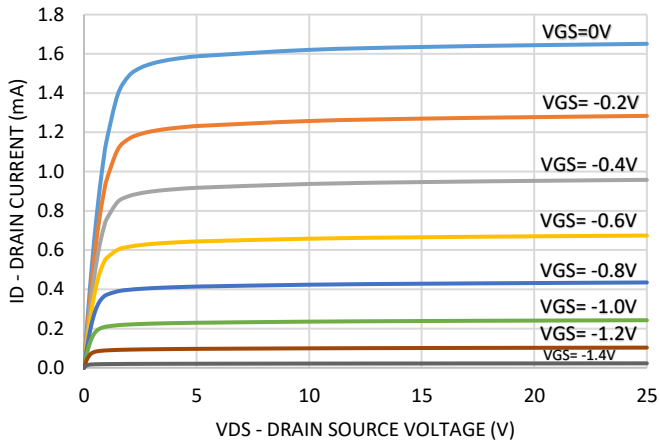
SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
g_{fs}	Forward Transconductance	J/SST201, 204	0.5			mS	V_{DS} = 15V, V_{GS} = 0.0V, *f* = 1kHz
		J/SST202	1.0				
C_{iss}	Input Capacitance			4.5		pF	V_{DS} = 15V, V_{GS} = 0.0V, *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance			1.3			
e_n	Noise Voltage			4.0		nV/√Hz	V_{DS} = 10V, V_{GS} = 0.0V, *f* = 1kHz

Typical Characteristics

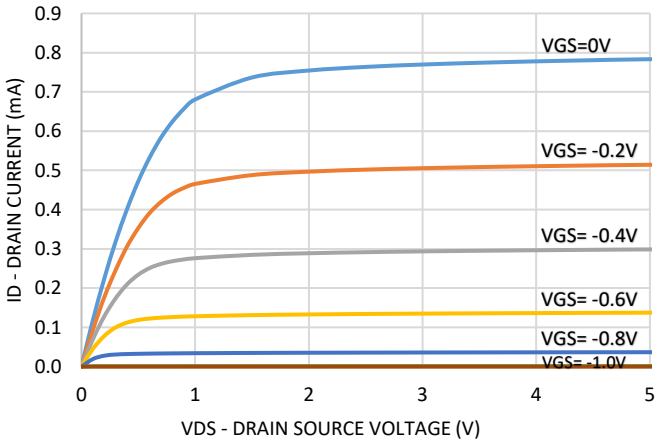
Output Characteristic
J201 - (VGS(off) = -1.1V)



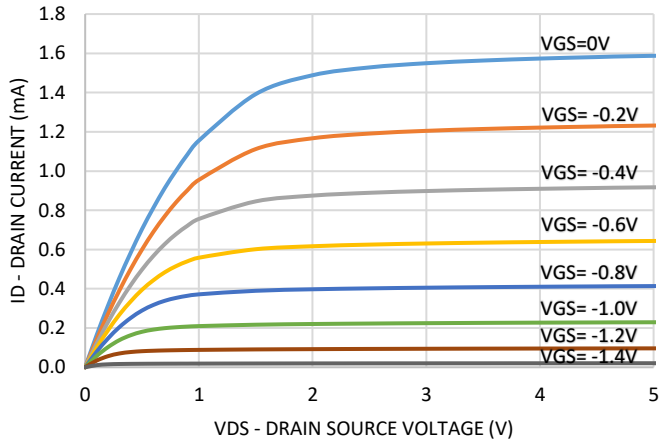
Output Characteristic
J202 - (VGS(off) = -1.75V)



Output Characteristic
J201 - (VGS(off) = -1.1V)

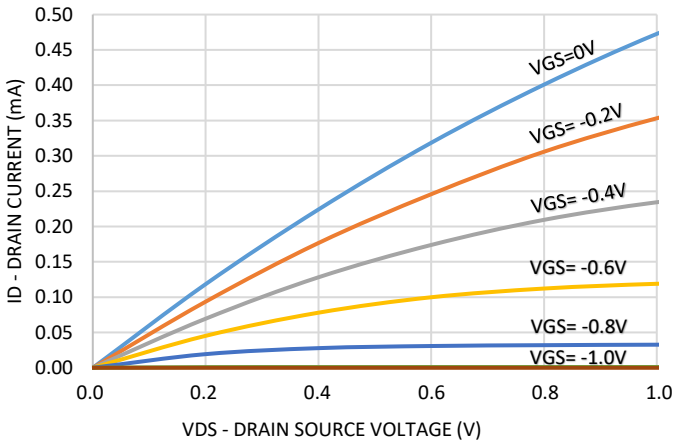


Output Characteristic
J202 - (VGS(off) = -1.75V)

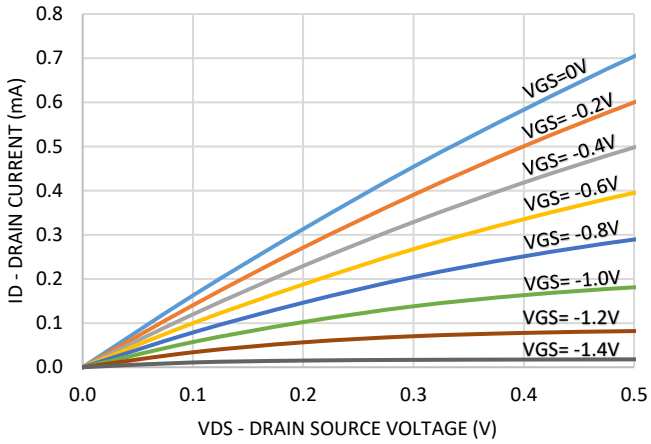


Typical Characteristics Continued

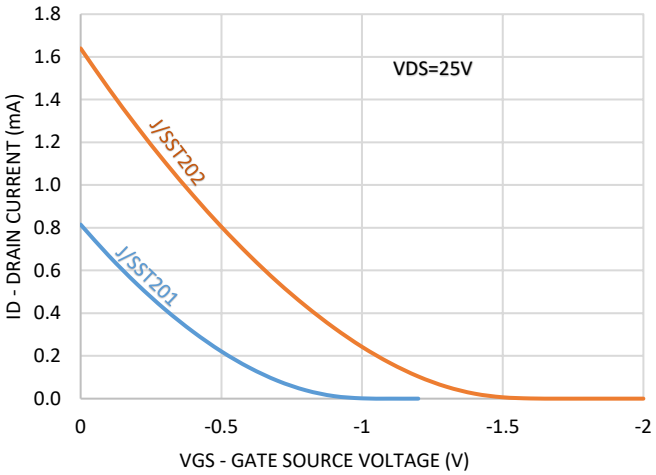
Output Characteristic
J201 - (VGS(off) = -1.1V)



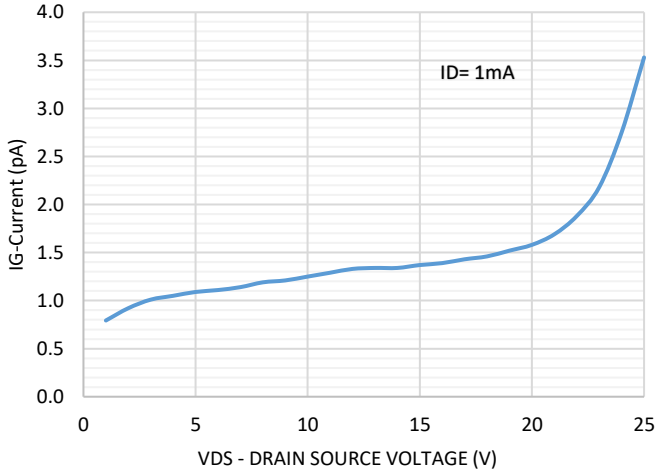
Output Characteristic
J202 - (VGS(off) = -1.75V)



Transfer Characteristics

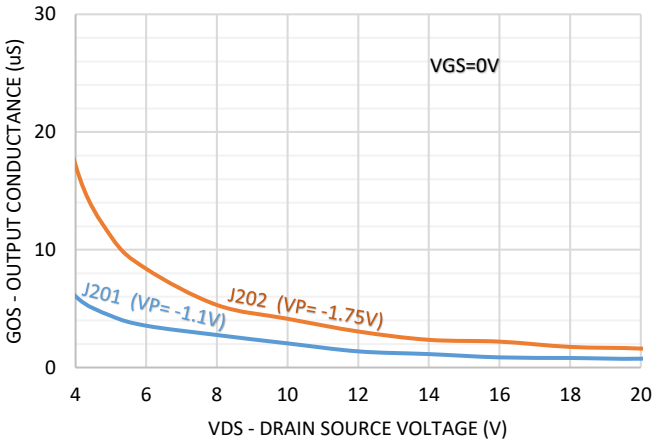


Operating Gate Current

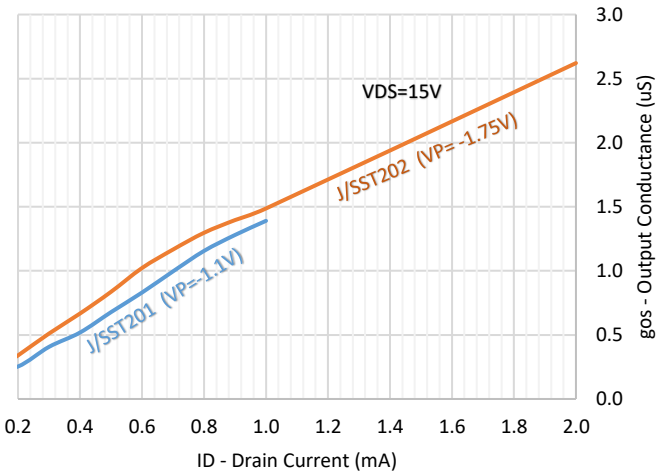


Typical Characteristics Continued

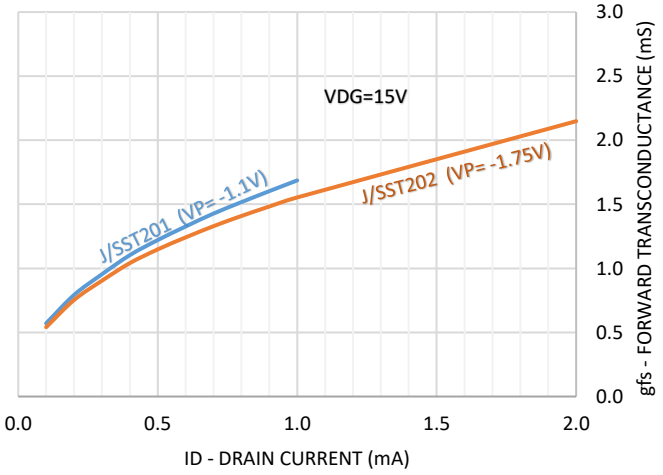
Output Conductance vs Drain Source Voltage



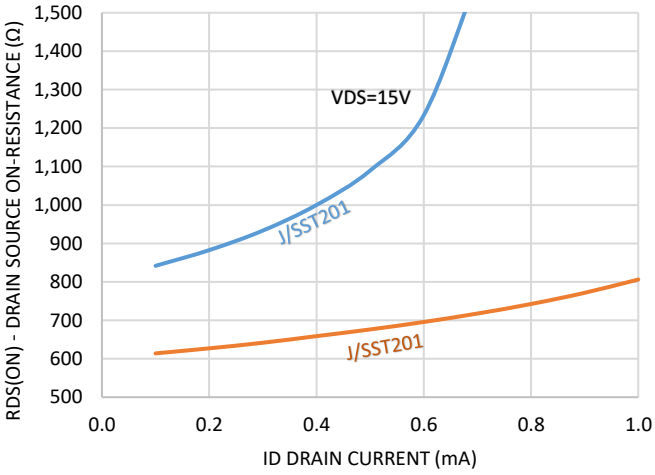
Output Conductance vs. Drain Current



Forward Transconductance vs. Drain Current

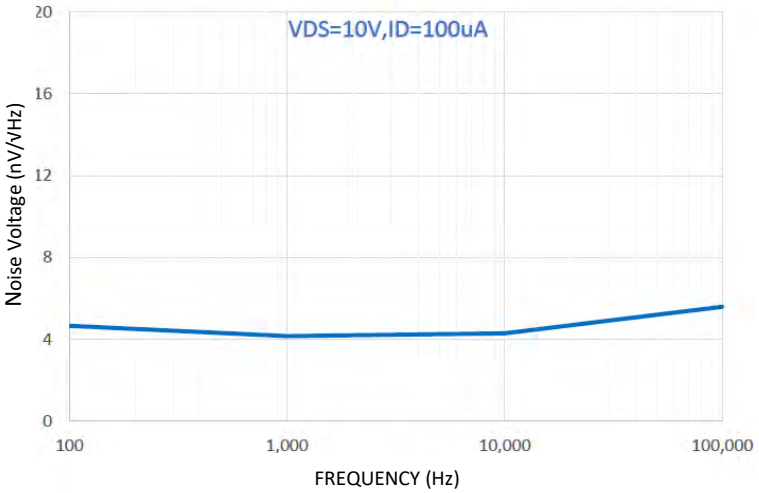


RDS - ID

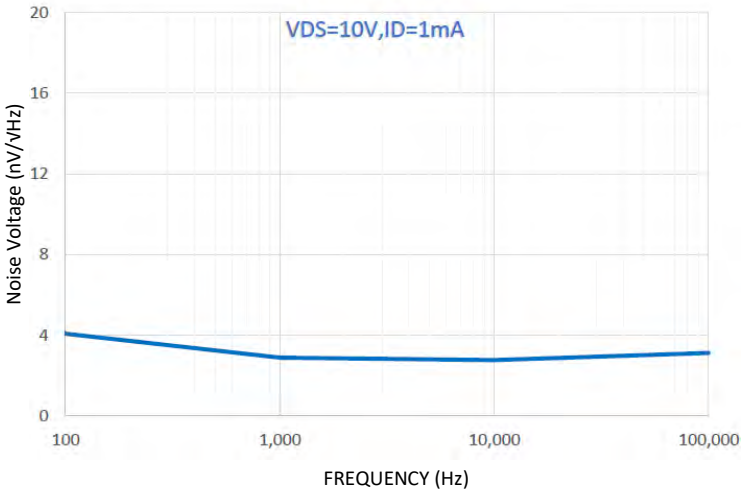


Typical Characteristics Continued

Input Noise Voltage vs Frequency

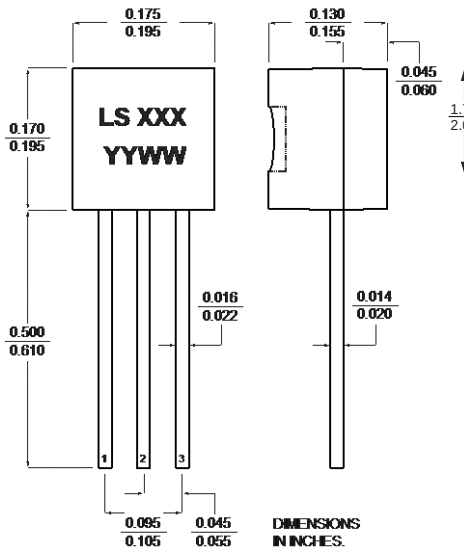


Input Noise Voltage vs Frequency

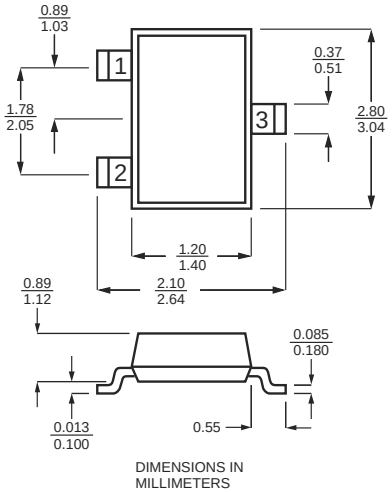


Package Dimensions

TO-92 3 Lead



SOT-23 3 Lead



Ordering Information

STANDARD PART CALL-OUT
J201 TO-92 3L RoHS
J202 TO-92 3L RoHS
J204 TO-92 3L RoHS
SST201 SOT-23 3L RoHS
SST202 SOT-23 3L RoHS
SST204 SOT-23 3L RoHS
CUSTOM PART CALL-OUT
(CUSTOM PARTS INCLUDE SEL + 4 DIGIT NUMERIC CODE)
J201 TO-92 3L RoHS SELXXXX
J202 TO-92 3L RoHS SELXXXX
J204 TO-92 3L RoHS SELXXXX
SST201 SOT-23 3L RoHS SELXXXX
SST202 SOT-23 3L RoHS SELXXXX
SST204 SOT-23 3L RoHS SELXXXX

Notes

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.
4. When ordering include the full Linear Systems part number and package type. Linear Systems creates custom parts on a case by case basis. To learn whether Linear Systems can meet your requirements, please send your drawing along with a detailed description of the device specifications to sales@linearsystems.com. One of our qualified representatives will contact you.
5. All standard parts are RoHS compliant. Contact the factory for availability of non-RoHS parts.
6. Information furnished by Linear Integrated Systems is believed to be accurate and reliable. However, no responsibility is assumed for its use; nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Linear Integrated Systems.

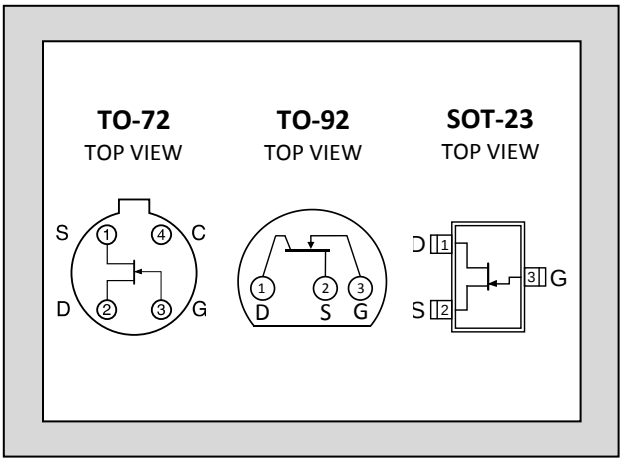
LINEAR SYSTEMS

Over Three Decades of Quality Through Innovation

LS846

LOW NOISE LOW LEAKAGE SINGLE N-CHANNEL JFET AMPLIFIER

FEATURES	
ULTRA LOW NOISE	e_n = 3nV/√Hz
LOW INPUT CAPACITANCE	C_{ISS} = 4pF
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Operating Junction Temperature	-55 to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation TA=25°C	300mW[3]
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSO} = 60V
Gate to Drain	V_{GDO} = 60V

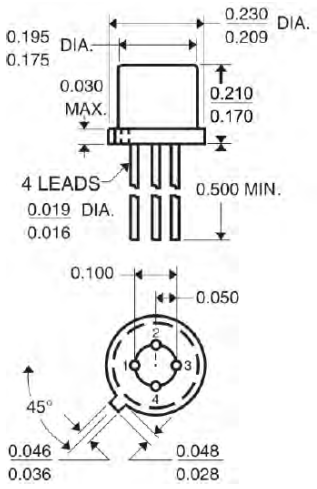


*For equivalent Monolithic Dual, see LS843 Family

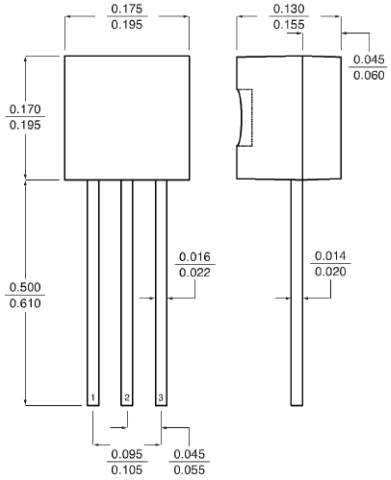
SYMBOL	CHARACTERISTIC[2]	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-60			V	V_{DS} = 0, I_D = 1nA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-1		-3.5	V	V_{DS} = 15V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage	-0.5		-3.5	V	V_{DS} = 15V, I_D = 500µA
I_{DSS}	Drain to Source Saturation Current	1.5	5	15	mA	V_{DS} = 15V, V_{GS} = 0
I_G	Gate Operating Current		-15	-50	pA	V_{DG} = 15V, I_D = 500µA
I_G	Gate Operating Current Reduced V_{DG}		-5	-30	pA	V_{DG} = 3V, I_D = 500µA
I_{GSS}	Gate to Source Leakage Current			-100	pA	V_{GS} = 15V, V_{DS} = 0
G_{fss}	Full Conductance Transconductance	1500			µS	V_{DS} = 15V, V_{GS} = 0, *f* = 1kHz
G_{fs}	Typical Operation Transconductance	1000	1500		µS	V_{DS} = 15V, I_D = 200µA
G_{OSS}	Full Output Conductance			40	µS	V_{DS} = 15V, V_{GS} = 0
G_{OS}	Typical Operation Output Conductance		2.0	2.70	µS	V_{DS} = 15V, I_D = 200µA
NF	Noise Figure			0.5	dB	V_{DS} = 15V, V_{GS} = 0, R_G = 10MΩ, *f* = 100Hz, NBW = 6Hz
e_n	Noise Voltage		3	7	nV/√Hz	V_{DS} = 15V, I_D = 500µA, *f* = 1kHz, NBW = 1Hz
e_n	Noise Voltage			11	nV/√Hz	V_{DS} = 15V, I_D = 500µA, *f* = 10Hz, NBW = 1Hz
C_{ISS}	Common Source Input Capacitance		4	8	pF	V_{DS} = 15V, I_D = 500µA, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Cap.			3	pF	

STANDARD PACKAGE DIMENSIONS:

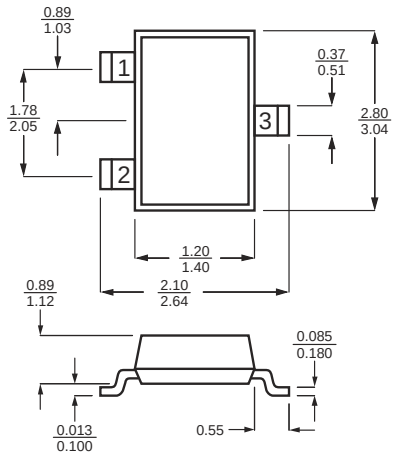
TO-72
Four Lead



TO-92
Three Lead



SOT-23
Three Lead



*Dimensions in inches

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicate negative electrical polarity only.
3. Derate 2.8mW/ºC above 25ºC.

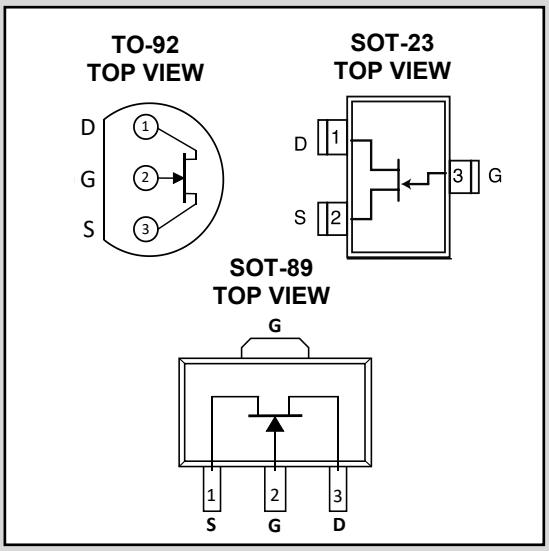
LINEAR SYSTEMS

Quality Through Innovation Since 1987

LSK170X-1

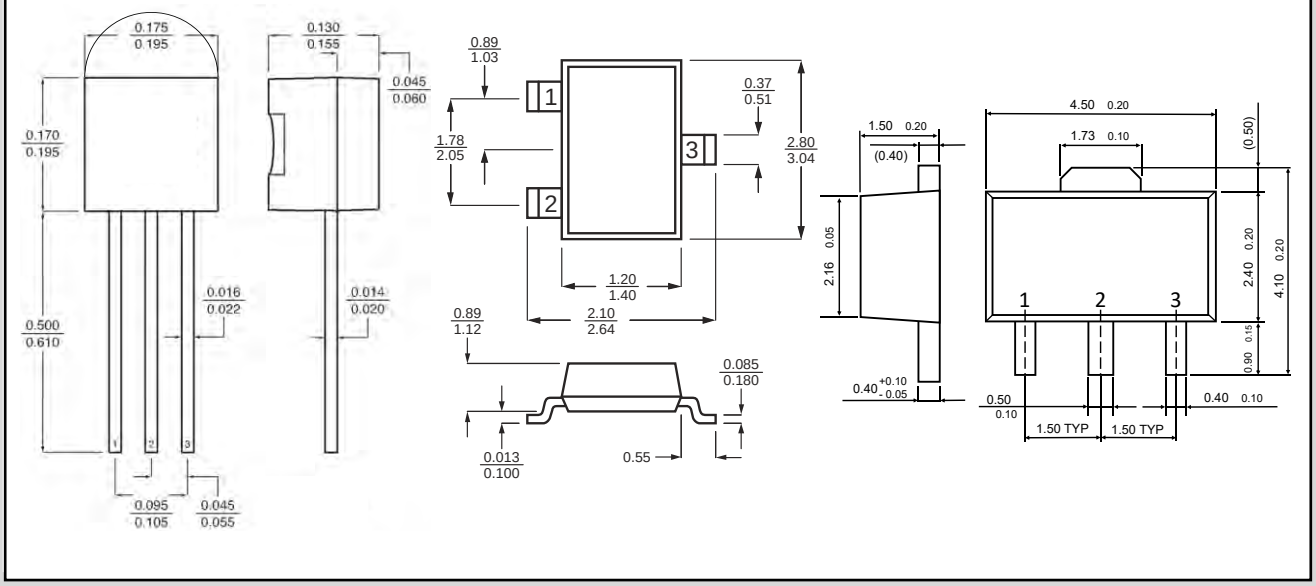
ULTRA LOW NOISE, HIGH IDSS SINGLE N-CHANNEL JFET AMPLIFIER

FEATURESss	
ULTRA LOW NOISE (f=1kHz)	e_n = 1.9NV/√HZ
HIGH BREAKDOWN VOLTAGE	BV_{GSS}=40V min
HIGH GAIN	G_{fs}=22mS (typ)
HIGH INPUT IMPEDENCE	I_G= -500pA max
LOW CAPACITANCE	20pF (typ)
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +135 °C
Maximum Power Dissipation	
Continuous Power Dissipation@+25°C	400mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$= 10mA
Maximum Voltages	
Gate to Source	V_{GS} = 40V
Gate to Drain	V_{GD} = 40V



ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-40			V	V_{DS} = 0, I_D = 100µA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-0.2		-2	V	V_{DS} = 10V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage		0.5		V	V_{DS} = 10V, I_D = 1mA
I_{DSS2}	Drain to Source Saturation Current	20		50	mA	V_{DS} = 10V, V_{GS} = 0
I_G	Gate Operating Current			-0.5	nA	V_{DG} = 10V, I_D = 1mA
I_{GSS}	Gate to Source Leakage Current			-1	nA	V_{GS} = -10V, V_{DS} = 0
G_{fS}	Full Conduction Transconductance		22		mS	V_{GD} = 10V, V_{GS} = 0, *f* = 1kHz
G_{fS}	Typical Conduction Transconductance		10		mS	V_{DG} = 15V, I_D = 1mA
e_n	Noise Voltage		1.9		nV/√Hz	V_{DS} = 10V, I_D = 2mA, *f* = 1kHz, NBW=1Hz
e_n	Noise Voltage		4.0		nV/√Hz	V_{DS} = 10V, I_D = 2mA, *f* = 10 Hz, NBW=1Hz
C_{ISS}	Common Source Input Capacitance		20		pF	V_{DS} = 15V, I_D = 100µA, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Cap.		5		pF	



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300μs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

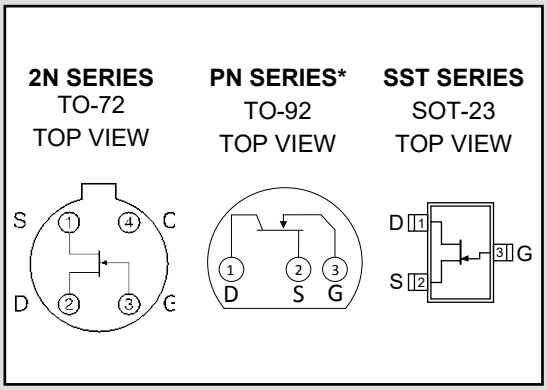
LINEAR SYSTEMS

Improved Standard Products®

2N/PN/SST4416 & 4416A

N-CHANNEL JFET HIGH FREQUENCY AMPLIFIER

FEATURES	
Replacement For SILICONIX 2N/SST4416 & 2N4416A	
VERY LOW NOISE FIGURE (400 MHz)	4 dB
EXCEPTIONAL GAIN (400 MHz)	10 dB
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +135 °C
Maximum Power Dissipation	
Continuous Power Dissipation	300mW
Maximum Currents	
Gate Current	10mA
Maximum Voltages	
Gate to Drain or Gate to Source 2N4416	-30V
Gate to Drain or Gate to Source 2N4416A	-35V



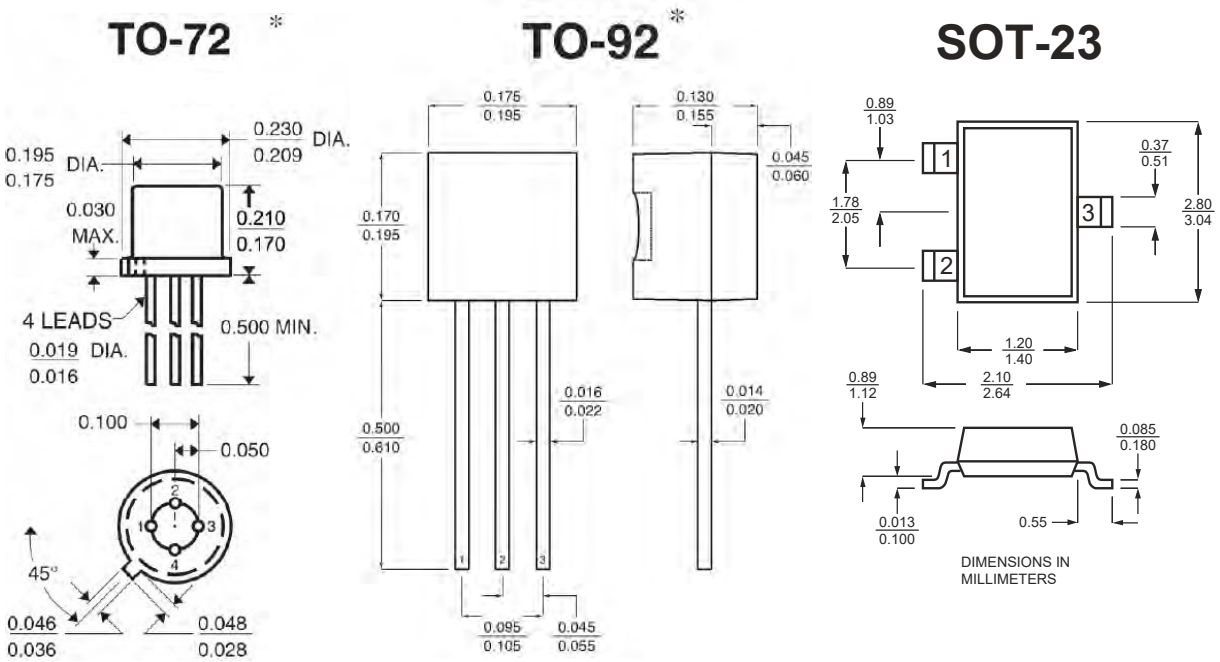
*Optional Package for 2N4416

ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	2N/PN/SST4416	-30			V	I_G = -1µA, V_{DS} = 0V
		2N4416A	-35				
$V_{GS(off)}$	Gate to Source Cutoff Voltage	2N/PN/SST4416			-6		V_{DS} = 15V, I_D = 1nA
		2N4416A	-2.5		-6		
I_{DSS}	Gate to Source Saturation Current		5		15	mA	V_{DS} = 15V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current	2N			-0.1	nA	V_{GS} = -20V, V_{DS} = 0V
		PN/SST			-1.0		V_{GS} = -15V, V_{DS} = 0V
g_{fs}	Forward Transconductance		4000		7500	µS	V_{DS} = 15V, V_{GS} = 0V, *f* = 1kHz
g_{os}	Output Conductance				100		
C_{iss}	Input Capacitance[2]				0.8	pF	V_{DS} = 15V, V_{GS} = 0V, *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance[2]				4		
C_{oss}	Output Capacitance[2]				2		
e_n	Equivalent Input Noise Voltage			6		nV/√Hz	V_{DS} = 10V, V_{GS} = 0V, *f* = 1kHz

HIGH FREQUENCY ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	100 MHz		400 MHz		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
g_{iss}	Input Conductance[2]		100		1000	μS	V_{DS} = 15V, V_{GS} = 0V
b_{iss}	Input Susceptance[2]		2500		10000		
g_{oss}	Output Conductance[2]		75		100		
b_{oss}	Output Susceptance[2]		1000		4000		
G_{fs}	Forward Transconductance[2]			4000			
G_{ps}	Power Gain[2]	18		10		dB	V_{DS} = 15V, I_D = 5mA
NF	Noise Figure[2]		2		4		V_{DS} = 15V, I_D = 5mA, R_G = 1kΩ



*Dimensions in Inches

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Not production tested, guaranteed by design.

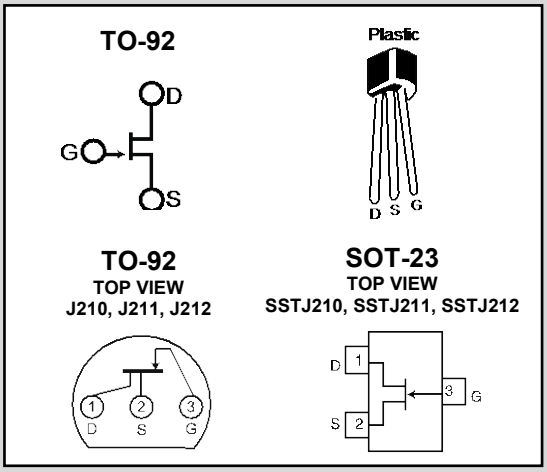
LINEAR SYSTEMS

Improved Standard Products®

SST/J210, 211 & 212

LOW NOISE N-CHANNEL JFET GENERAL PURPOSE AMPLIFIER

FEATURES	
HIGH GAIN g_{fs}=7000µmho MINIMUM (J211, J212)	
HIGH INPUT IMPEDENCE I_{GSS}= 100pA MAXIMUM	
LOW CAPACITANCE C_{ISS}= 5pF TYPICAL	
ABSOLUTE MAXIMUM RATINGS @ 25 °C (unless otherwise stated)	
Gate-Drain or Gate-Source Voltage	-25V
Gate Current	10mA
Total Device Dissipation @25°C Ambient (Derate 3.27 mW/°C)	360mW
Operating Temperature Range	-55 to +150 °C



ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTICS	SSTJ210			SSTJ211			SSTJ212			UNITS	CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{GSS}	Gate Reverse Current	--	--	-100	--	--	-100	--	--	-100	pA	V_{DS} = 0, V_{GS} = -15V (NOTE 1)	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	--	-3	-2.5	--	-4.5	-4	--	-6	V	V_{DS} = 15V, I_D = 1nA	
BV_{GSS}	Gate-Source Breakdown Voltage	-25	--	--	-25	--	--	-25	--	--		V_{DS} = 0, I_G = -1µA	
I_{DSS}	Drain Saturation Current	2	--	15	7	--	20	15	--	40	mA	V_{DS} = 15V, V_{GS}=0 (NOTE 2)	
I_G	Gate Current	--	-10	--	--	-10	--	--	-10	--	pA	V_{DS} = 10V, I_D=1mA (NOTE 1)	
g_{fs}	Common-Source Forward Transconductance	4,000	--	12,000	6,000	--	12,000	7,000	--	12,000	µmho	V_{DS} = 15V, V_{GS}=0	f=1kHz
g_{os}	Common-Source Output Conductance	--	--	150	--	--	200	--	--	200			
C_{ISS}	Common-Source Input Capacitance	--	4	--	--	4	--	--	4	--	pF		f=1MHz
C_{rss}	Common-Source Reverse Transfer Capacitance	-	1	--	--	1	--	--	1	--			
e_n	Equivalent Short-Circuit Input Noise Voltage	-	10	--	--	10	--	--	10	--	nV√Hz		f=1kHz

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2ms.

LINEAR SYSTEMS

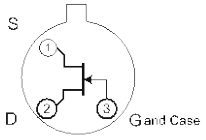
Improved Standard Products®

U/J/SST308 SERIES

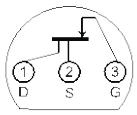
SINGLE N-CHANNEL, HIGH FREQUENCY JFET AMPLIFIER

FEATURES	
Direct Replacement For SILICONIX U/J/SST308 SERIES	
OUTSTANDING HIGH FREQUENCY GAIN	G_{pg} = 11.5dB
LOW HIGH FREQUENCY NOISE	NF = 2.7dB
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to 150°C
Junction Operating Temperature	-55 to 150°C
Maximum Power Dissipation	
Continuous Power Dissipation (J/SST)[4]	350mW
Continuous Power Dissipation (U)[5]	500mW
Maximum Currents	
Gate Current (J/SST)	10mA
Gate Current (U)	20mA
Maximum Voltages	
Gate to Drain	-25V
Gate to Source	-25V

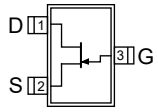
U SERIES
TO-18
TOP VIEW



J SERIES
TO-92
TOP VIEW



SST SERIES
SOT-23
TOP VIEW



COMMON ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNIT	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage		-25			V	I_G = -1µA, V_{DS} = 0V
$V_{GS(F)}$	Gate to Source Forward Voltage		0.7		1.15		I_G = 10mA, V_{DS} = 0V
I_G	Gate Operating Current			-15		pA	V_{DG} = 9V, I_D = 10mA
$r_{DS(on)}$	Drain to Source On Resistance			35		Ω	V_{GS} = 0V, I_D = 1mA
e_n	Equivalent Noise Voltage			6		nV/√Hz	V_{DS} = 10V, I_D = 10mA, *f* = 100Hz
NF	Noise Figure	*f* = 105MHz		1.5		dB	V_{DS} = 10V, I_D = 10mA
		f = 450MHz		2.7			
G_{pg}	Power Gain[2]	*f* = 105MHz		16			
		f = 450MHz		11.5			
g_{fg}	Forward Transconductance	*f* = 105MHz		14		mS	
		f = 450MHz		13			
g_{og}	Output Conductance	*f* = 105MHz		0.16			
		f = 450MHz		0.55			
IGSS	Gate Reverse Current				-1	nA	V_{GS} = -15V, V_{DS} = 0V

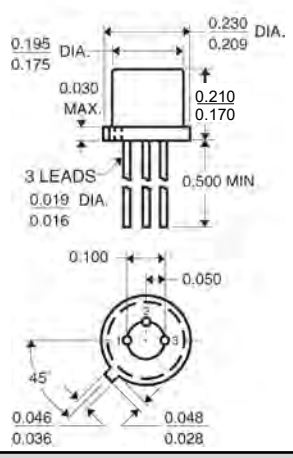
SPECIFIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	J/SST308		J/SST309		J/SST310		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
$V_{GS(off)}$	Gate to Source Cutoff Voltage		-1	-6.5	-1	-4	-2	-6.5	V	V_{DS} = 10V, I_D = 1nA
I_{DSS}	Source to Drain Saturation Current[3]		12	75	12	30	24	75	mA	V_{DS} = 10V, V_{GS} = 0V
C_{iss}	Input Capacitance	4							pF	V_{DS} = 10V, V_{GS} = -10V *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance	1.9								
g_{fs}	Forward Transconductance	14	8		10		8		mS	V_{DS} = 10V, I_D = 10mA *f* = 1kHz
g_{os}	Output Conductance	110		250		250		250	µS	

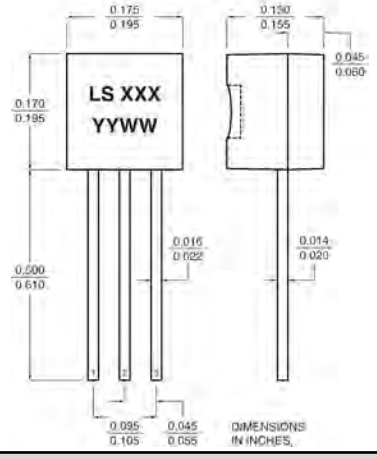
SPECIFIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	U308		U309		U310		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
$V_{GS(off)}$	Gate to Source Cutoff Voltage		-1	-6.5	-1	-4	-2.5	-6.5	V	V_{DS} = 10V, I_D = 1nA
I_{DSS}	Source to Drain Saturation Current[3]		12	75	12	30	24	75	mA	V_{DS} = 10V, V_{GS} = 0V
C_{iss}	Input Capacitance	4		5		5		5	pF	V_{DS} = 10V, V_{GS} = -10V *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance	1.9		2.5		2.5		2.5		
g_{fs}	Forward Transconductance	14	10		10		10		mS	V_{DS} = 10V, I_D = 10mA *f* = 1kHz
g_{os}	Output Conductance	110		250		250		250	µS	

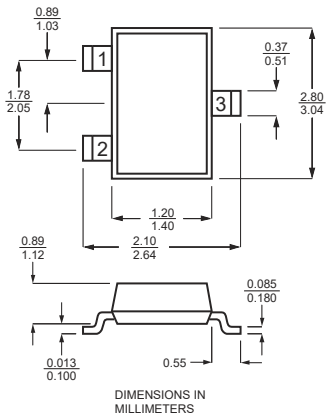
TO-18



TO-92



SOT-23



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Measured at optimum input noise match
3. Pulse test: PW ≤ 300µs, Duty Cycle ≤ 3%
4. Derate 2.8mW/ºC above 25ºC
5. Derate 4mW/ºC above 25ºC

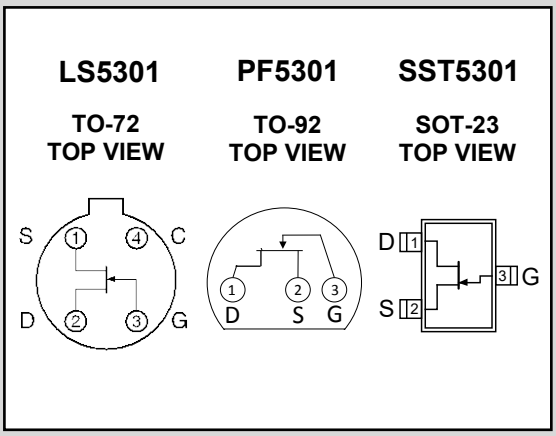
LINEAR SYSTEMS

Improved Standard Products®

LS5301/PF5301/ SST5301

VERY HIGH INPUT IMPEDANCE N-CHANNEL JFET AMPLIFIER

Features	
Replacement for LF5301, PF5301	
High Input Impedance	I_G >1 GΩ
High Gain	g_{fs} > 70 µS
Absolute Maximum Ratings[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures (°C)	
Storage Temperature	-55 to 150°C
Operating Junction Temperature	-55 to 135°C
Maximum Power Dissipation @TA = 25°C	**300mW**
Derate LS5301	2.0mW/°C
Derate PF & SST5301	2.8mW/°C
Maximum Forward Current	**50mA**
Maximum Gate to Drain Voltage	**-30V**
Maximum Gate to Source Voltage	**-30V**



Static Electrical Characteristics @ TA = 25°C (unless otherwise stated)

Symbol	Characteristic			TYP	Max	Unit	Conditions
BV_{GSS}	Gate to Source Breakdown Voltage		-30			V	V_{DS} = 0V, I_D = -1µA
$V_{GS(off)}$	Gate to Source Cutoff Voltage		-0.6		-3.0		V_{DS} = 10V, I_D = 1nA
I_{GSS}	Gate Leakage Current	LS5301			-1	pA	V_{DS} = 15V, V_{GS} = 0V
		PF5301			-5		
		SST5301			-10		
I_G	Gate Operating Current			-0.04			V_{DG} = 6V, I_D = 5µA
I_{DSS}	Drain to Source Saturation Current		30		500	µA	V_{DS} = 10V, V_{GS} = 0V
g_{fs}	Forward Transconductance		70		500	µS	V_{DS} = 10V, V_{GS} = 0V, *f* = 1kHz
C_{iss}	Input Capacitance				3	pF	V_{DS} = 10V, V_{GS} = 0V, *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance				1.5		
e_n	Equivalent Noise Voltage			45	150	nV/√Hz	V_{DG} = 10V, I_D = 50µA, *f* = 100Hz

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Derate PF series 2.8mW/° C when TA>25° C. Derate LS series 2.0mW°C when TA>25° C
3. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicated electrical polarity only.

LINEAR SYSTEMS

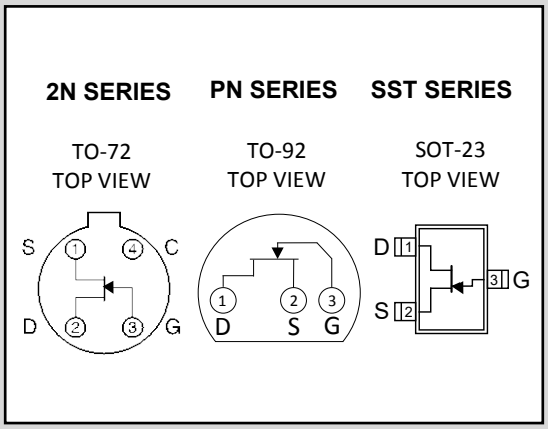
Improved Standard Products®

2N/PN/SST 4117, 4118, 4119

ULTRA-HIGH INPUT IMPEDANCE N-CHANNEL JFET AMPLIFIER

FEATURES	
LOW POWER	I_{DSS}<600 µA (2N4117A)
MINIMUM CIRCUIT LOADING	I_{GSS}<1 pA (2N4117A Series)

ABSOLUTE MAXIMUM RATINGS (NOTE 3) @ 25°C (unless otherwise noted)	
Gate-Source or Gate-Drain Voltage	-40V
Gate-Current	50mA
Total Device Dissipation (Derate 2mW/ºC above 25ºC)	300mW
Storage Temperature Range	-55ºC to+150ºC
Lead Temperature (1/16" from case for 10 seconds)	300ºC



ELECTRICAL CHARACTERISTICS @ 25ºC (unless otherwise noted)

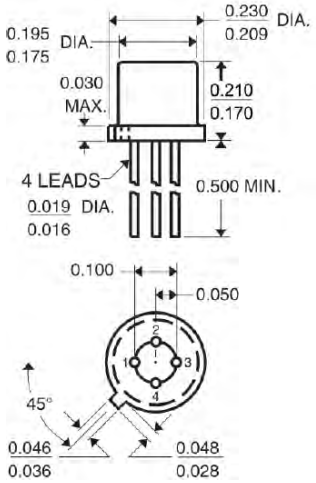
SYMBOL	CHARACTERISTIC	4117 MIN	4117 MAX	4118 MIN	4118 MAX	4119 MIN	4119 MAX	UNITS	CONDITIONS	
BV_{GSS}	Gate-Source Breakdown Voltage	-40	--	-40	--	-40	--	V	I_G =-1µA V_{DS}=0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-1.8	-1	-3	-2	-6		V_{DS} =10V I_D=1nA	
I_{DSS}	Saturation Drain Current (NOTE 2)	0.03	0.60	0.08	0.60	0.20	0.80	mA	V_{DS} =10V V_{GS}=0	
I_{GSS}	Gate Reverse Current 2N4117A, 2N4118A, 2N4119A	--	-1	--	-1	--	-1	pA	V_{GS} =-20V V_{DS}=0	
		--	-2.5	--	-2.5	--	-2.5	nA		150ºC
	PN4117, PN4118, PN4119 SST4117, SST4118, SST4119	--	-10	--	-10	--	-10	pA	V_{GS} =-10V V_{DS}=0	
		--	-25	--	-25	--	-25	nA		150ºC
g_{fs}	Common-Source Forward Transconductance	70	450	80	650	100	700	µS	V_{DS} =10V V_{GS}=0	f=1kHz
g_{os}	Common-Source Output Conductance	--	3	--	5	--	10			
C_{iss}	Common-Source Input Capacitance (NOTE 4)	--	3	--	3	--	3	pF		f=1MHz
C_{rss}	Common-Source Reverse Transfer Capacitance (NOTE 4)	--	1.5	--	1.5	--	1.5			

STANDARD PACKAGE DIMENSIONS:

2N4117A, 2N4118A, 2N4119A

TO-72

Three Lead

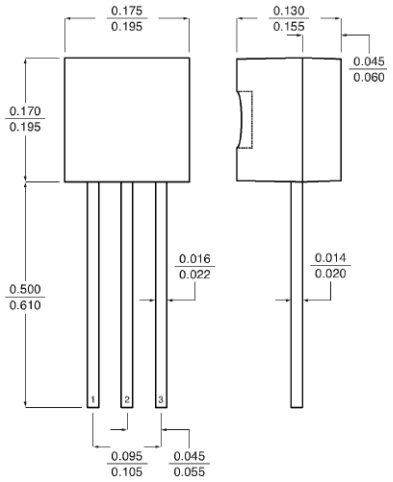


*Dimensions in inches

PN4117, PN4118, PN4119

TO-92

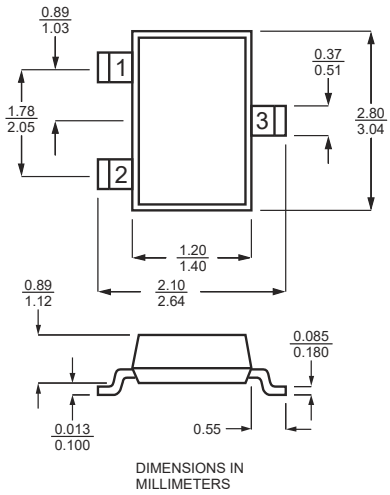
Three Lead



SST4117, SST4118, SST4119

SOT-23

Three Lead



NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)
3. Absolute maximum ratings are limiting values above which serviceability may be impaired.
4. Not production tested, guaranteed by design.

LINEAR SYSTEMS

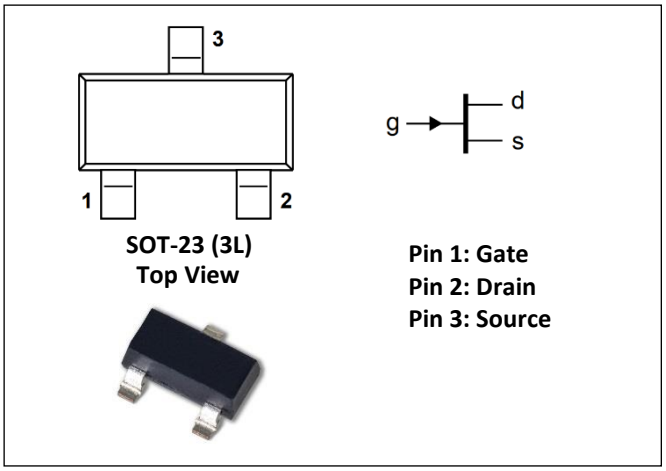
Improved Standard Products®

LSBF510

High Gain, Single N-Channel JFET Amplifier

General Purpose, Low-Noise, Low-Cost, Single N-Channel JFET, Replacement for the BF510

Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation @ +25°C	350mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = 30V
Gate to Drain	V_{GDS} = 30V



Features

- Low Cutoff Voltage: <2.5V
- High Input Impedance
- Very Low Noise
- High Gain: AV = 80 @ 20 µA
- Reverse Gate to Source and Drain Voltage ≥| -30V

Benefits

- Low Cost
- Excellent Low Power Supply Operation
- Power Supply: Down to 2.5V
- Low Signal Loss/System Error
- High System Sensitivity
- High Quality Low-Level Signal

Applications

- High-Gain, Low Noise Amplifiers
- Low-Current, Low-Voltage
- Battery-Powered Amplifiers
- Infrared Detector Amplifiers
- Ultra-High Input Impedance Pre-Amplifiers

Description

The LSBF510 is a low-cost N-Channel JFET. Features include low leakage, very low noise, low cutoff voltage ($V_{GS(off)} \leq 2.5V$) and high Gain (A_V = 80 V/V) for use with low-level power supplies. The LSBF510 is excellent for battery powered equipment and low current amplifiers. The TO-236 (SOT-23) package provides surface-mount capability. The LSBF510 is available in tape-and-reel for automated assembly and in die form for automated assembly.

Electrical Characteristics @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-30			V	I_G = -1µA, V_{DS} = 0.0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.3		-2.5		V_{DS} = 15V, I_D = 10nA
I_{DSS}	Drain to Source Saturation Current[2]	0.2		3.0	mA	V_{DS} = 15V, V_{GS} = 0.0V
I_{GSS}	Gate Reverse Current			-200	pA	V_{GS} = -20V, V_{DS} = 0.0V
I_G	Gate Operating Current		-2			V_{DG} = 10V, I_D = 0.1mA
$I_{D(off)}$	Drain Cutoff Current		2			V_{DS} = 15V, V_{GS} = 5.0V
g_{fs}	Forward Transconductance	0.5			mS	V_{DS} = 15V, V_{GS} = 0.0V, *f* = 1kHz
C_{iss}	Input Capacitance			4.5	pF	V_{DS} = 15V, V_{GS} = 0.0V, *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance		1.3			
e_n	Noise Voltage		3.0		nV/√Hz	V_{DS} = 10V, I_D = 2mA, *f* = 1kHz

Typical Characteristics

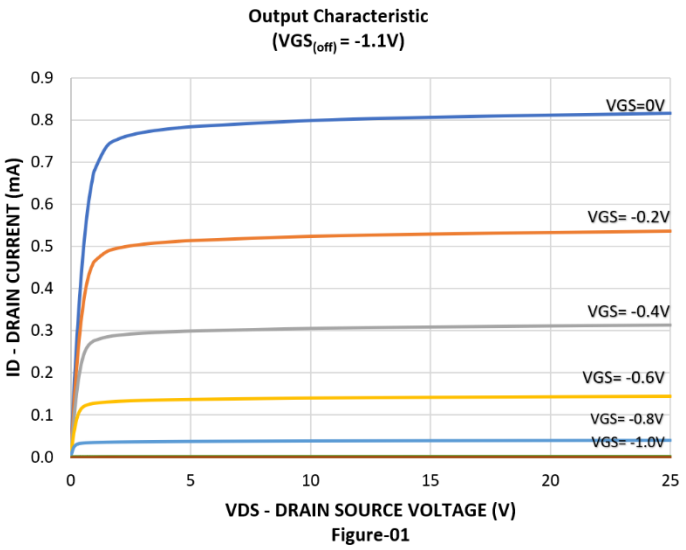


Figure-01

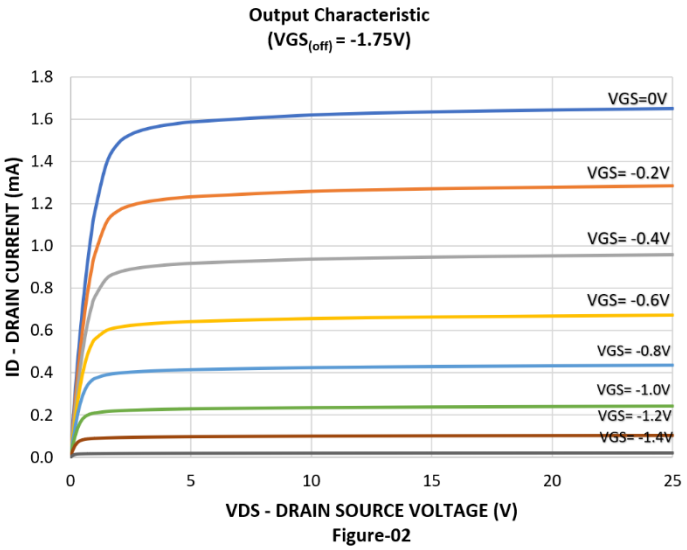


Figure-02

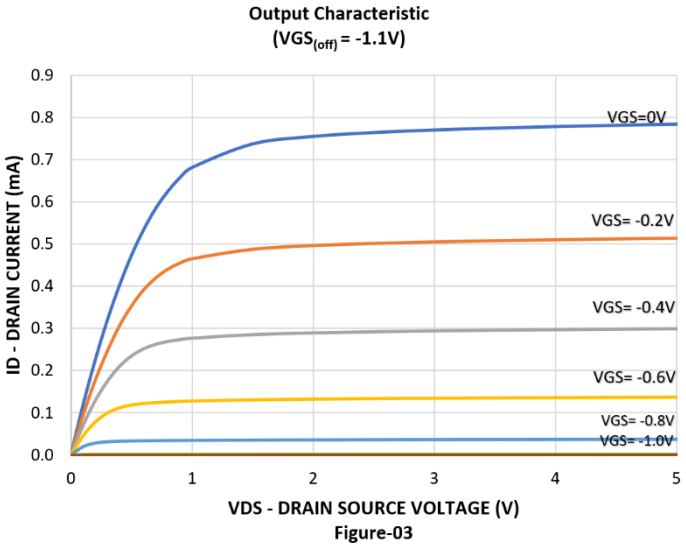


Figure-03

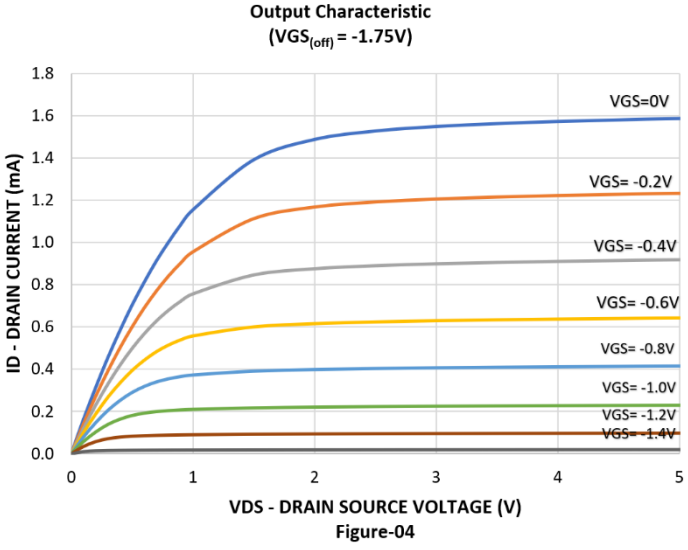


Figure-04

Typical Characteristics Continued

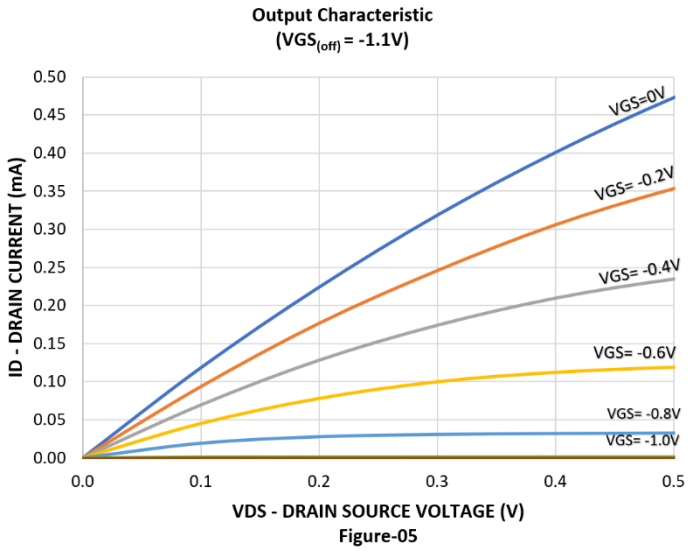


Figure-05

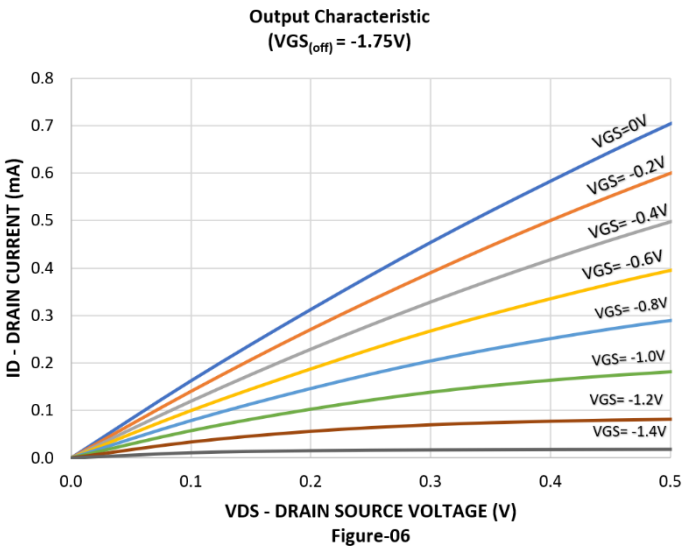


Figure-06

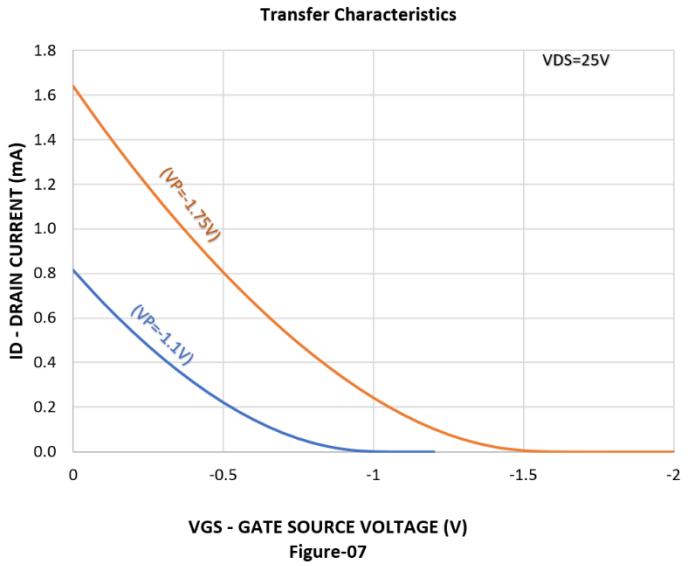


Figure-07

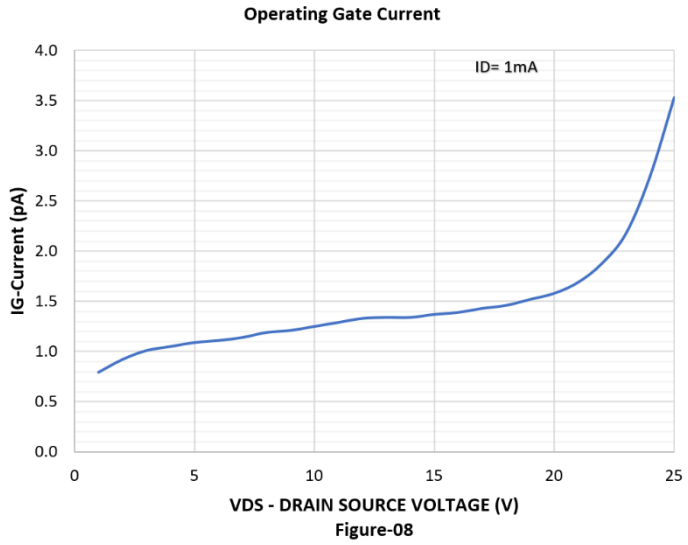


Figure-08

Typical Characteristics Continued

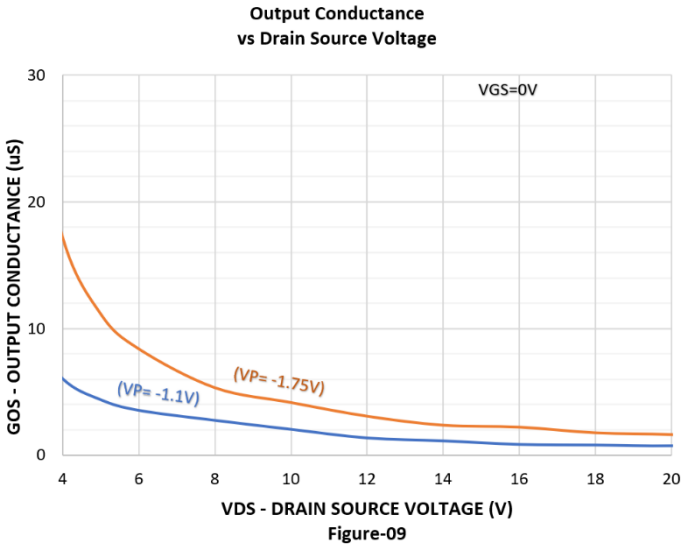


Figure-09

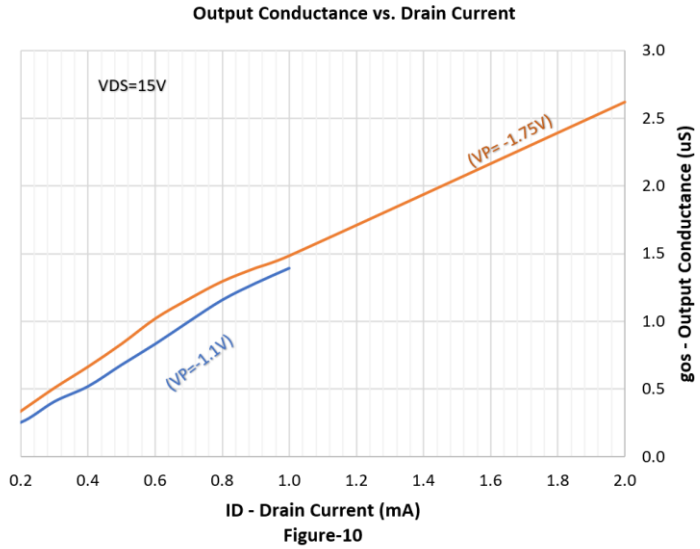


Figure-10

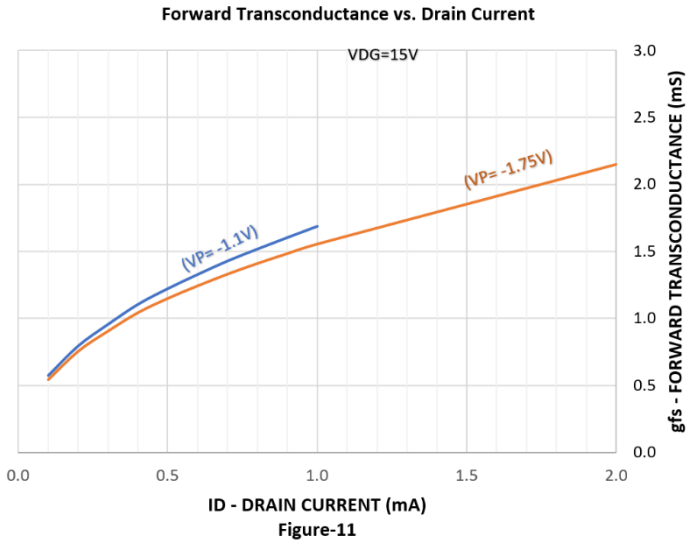


Figure-11

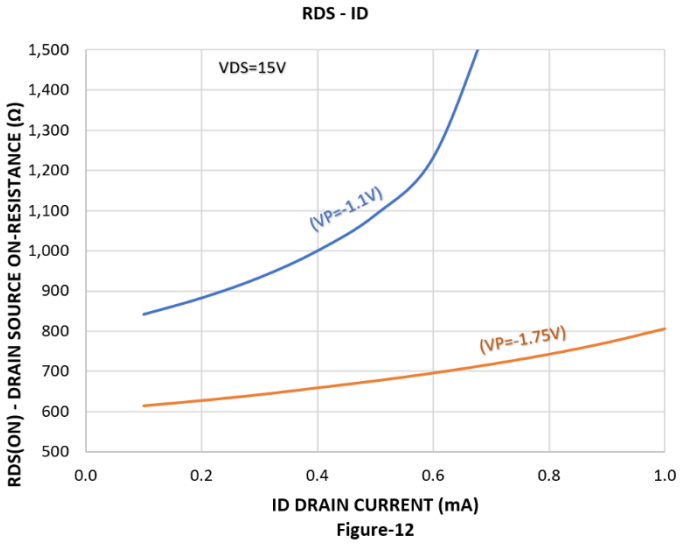
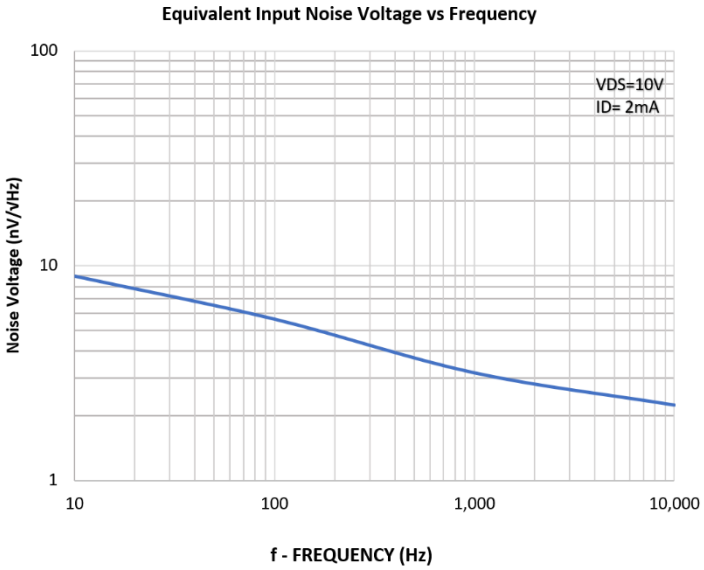


Figure-12

Typical Characteristics Continued



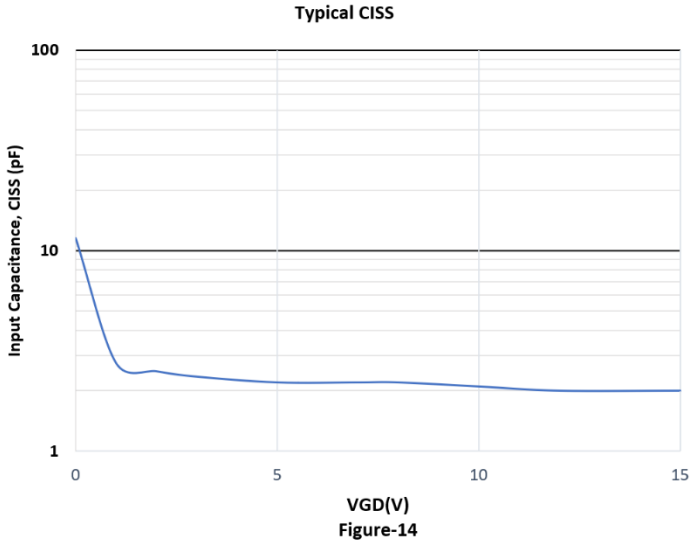
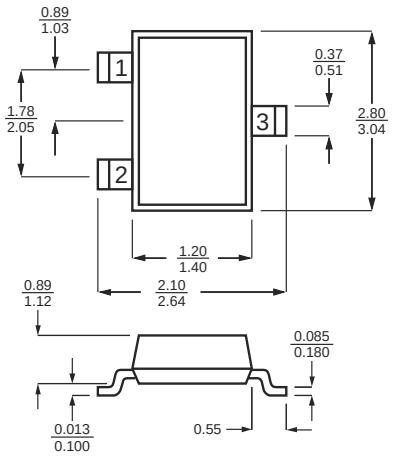


Figure-14

Package Dimensions

SOT-23 3 Lead



DIMENSIONS IN MILLIMETERS

Ordering Information

STANDARD PART CALL-OUT
LSBF510 SOT-23 3L RoHS
CUSTOM PART CALL-OUT
(CUSTOM PARTS INCLUDE SEL + 4 DIGIT NUMERIC CODE)
LSBF510 SOT-23 3L RoHS SELXXXX

Notes

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.
4. When ordering include the full Linear Systems part number and package type. Linear Systems creates custom parts on a case by case basis. To learn whether Linear Systems can meet your requirements, please send your drawing along with a detailed description of the device specifications to sales@linearsystems.com. One of our qualified representatives will contact you.
5. All standard parts are RoHS compliant. Contact the factory for availability of non-RoHS parts.
6. Information furnished by Linear Integrated Systems is believed to be accurate and reliable. However, no responsibility is assumed for its use; nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Linear Integrated Systems.

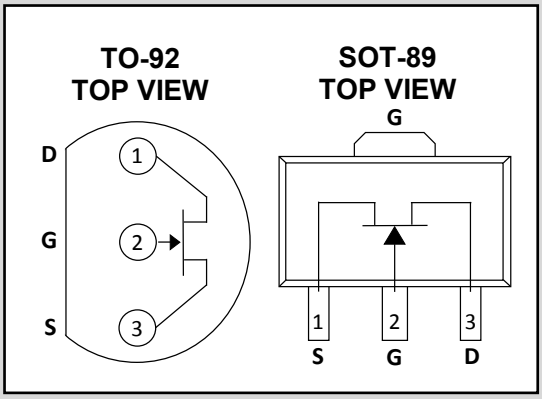
LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

LS190

GENERAL PURPOSE SINGLE N-CHANNEL JFET AMPLIFIER

FEATURES	
HIGH BREAKDOWN VOLTAGE	BV_{GSS}=40V max
HIGH GAIN	G_{fs}=22mS (typ)
HIGH INPUT IMPEDENCE	I_G= -500pA max
LOW CAPACITANCE	20pF (typ)
ABSOLUTE MAXIMUM RATINGS[1] TA = 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +135 °C
Maximum Power Dissipation	
Continuous Power Dissipation (TO-92)	400mW[4]
Continuous Power Dissipation (SOT-89)	1.4W[5, 6]
Maximum Currents	
Gate Forward Current	$I_{G(F)}$= 10mA
Maximum Voltages	
Gate to Source	V_{GS} = 40V
Gate to Drain	V_{GD} = 40V



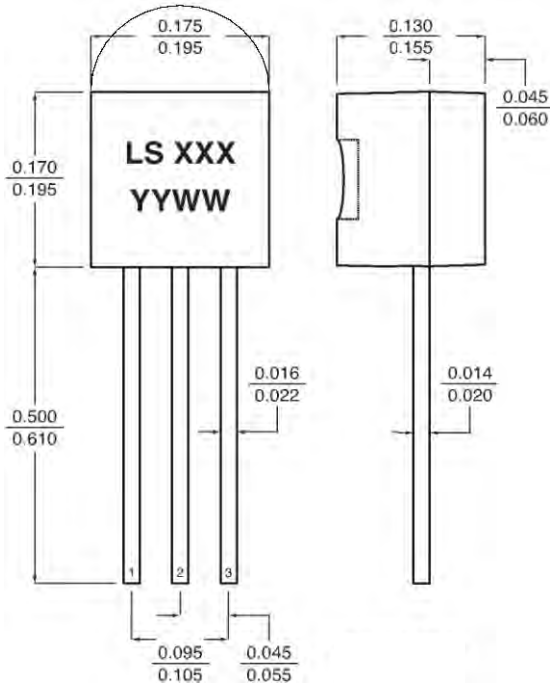
*For equivalent monolithic dual, see LSK589

ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-40			V	V_{DS} = 0, I_D = 100µA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-0.2		-2	V	V_{DS} = 10V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage		-0.5		V	V_{DS} = 10V, I_D = 1mA
I_{DSS}	Drain to Source Saturation Current	2.6		30	mA	V_{DS} = 10V, V_{GS} = 0
I_G	Gate Operating Current			-0.5	nA	V_{DG} = 10V, I_D = 1mA
I_{GSS}	Gate to Source Leakage Current			-1	nA	V_{GS} = -10V, V_{DS} = 0
G_{fS}	Full Conduction Transconductance		22		mS	V_{GD} = 10V, V_{GS} = 0, *f* = 1kHz
G_{fS}	Typical Conduction Transconductance		10		mS	V_{DG} = 15V, I_D = 1mA
$R_{DS(on)}$	Drain to Source on Resistance		75	150	Ω	V_{GS} = 0V, I_D = -1mA
C_{ISS}	Common Source Input Capacitance		20		pF	V_{DS} = 15V, I_D = 100µA, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Cap.		5		pF	

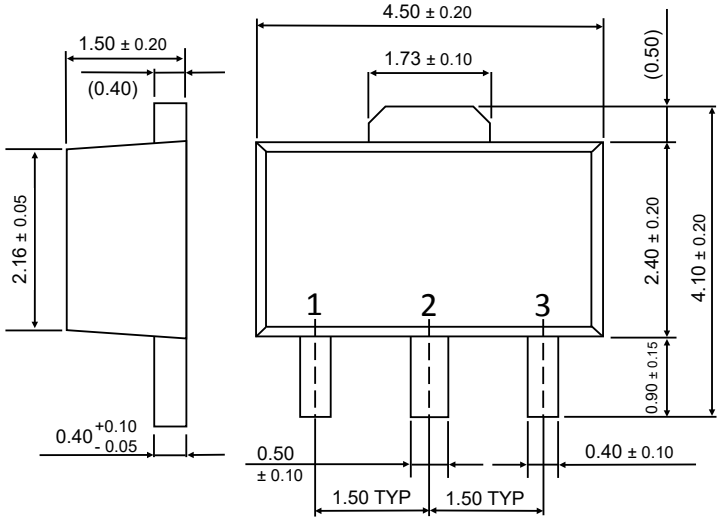
Standard Package Dimensions:

TO-92



Dimensions in inches

SOT-89



Dimensions in millimeters

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300μs, Duty Cycle ≤ 3%
3. Derate 2.8mW/ºC above TA = 25ºC
4. Mounted on FR5 board, 25mm x 25mm x 1.57mm
5. Derate by 25mW/ºC above 25ºC
6. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

LSJ689

LOW NOISE LOW CAPACITANCE MONOLITHIC DUAL P-CHANNEL JFET AMPLIFIER

FEATURES	
ULTRA LOW NOISE	e_n = 2.0nV/√Hz
LOW INPUT CAPACITANCE	Ciss = 8pF

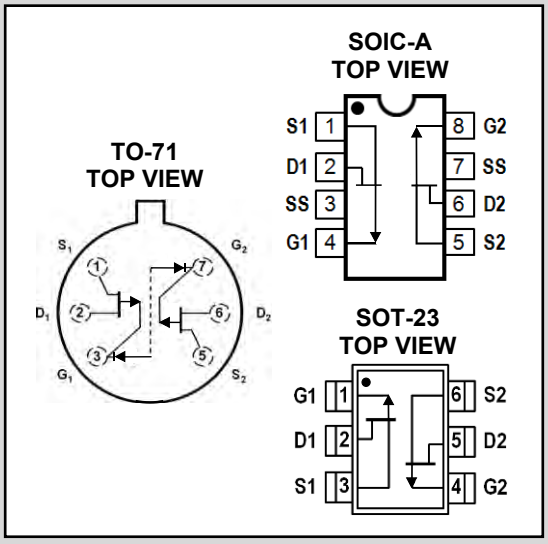
Features
- Reduced Noise due to process improvement
- Monolithic Design
- High slew rate
- Low offset/drift voltage
- Low gate leakage Igss & Ig
- High CMRR 102 dB

Benefits
- Tight differential voltage match vs. current
- Improved op amp speed settling time accuracy
- Minimum Input Error trimming error voltage
- Lower intermodulation distortion

Applications
- Wide band differential Amps
- High speed temperature compensated single ended input amplifier amps
- High speed comparators
- Impedance Converters

Description
The LSJ689 high performance, P-Channel, monolithic dual JFET features extremely low noise, tight offset voltage and low drift over temperature. It is targeted for use in a wide range of precision instrumentation applications. The SOT-23, TO-71 and SO-8 packages provide ease of manufacturing and the symmetrical pinouts prevent improper orientation. The SOT-23 and SO-8 packages are available in tape and reel, compatible with automatic assembly methods. (See packaging data)

ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation, TA = 25°C	
Continuous Power Dissipation, per side [4]	300mW
Power Dissipation, total [5]	500mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = -10mA
Maximum Voltages	
Gate to Source	V_{GS} = 50V
Gate to Drain	V_{GD} = 50V



MATCHING CHARACTERISTICS @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate to Source Voltage			20	mV	V_{DS} = -15V, I_G = -1mA
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.90		1.0		V_{DS} = -15V, V_{GS} = 0V
CMRR	**COMMON MODE REJECTION RATIO** $-20 \log \lvert \Delta V_{GS1-2} / \Delta V_{DS} \rvert$	95	102		db	V_{DS} = -10V to -20V, I_D = -200µA

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
e_n	Noise Voltage		1.9		nV/√Hz	V_{DS} = -15V, I_D = -2.0mA, *f* = 1kHz, NBW = 1Hz
e_n	Noise Voltage		2.2		nV/√Hz	V_{DS} = -15V, I_D = -2.0mA, *f* = 100Hz, NBW = 1Hz
C_{ISS}	Common Source Input Capacitance		8		pF	V_{DS} = -15V, I_D = -200µA, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Capacitance		3		pF	

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise stated)

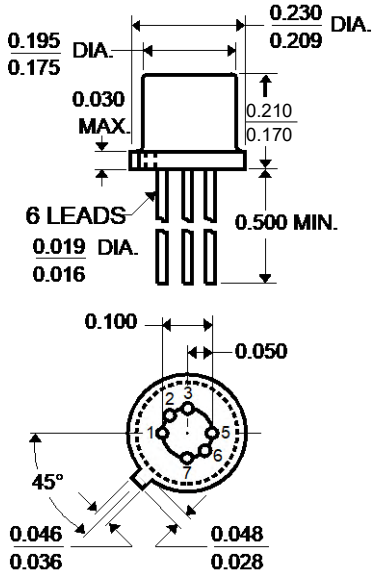
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	50			V	V_{DS} = 0V, I_G = 1µA
$V_{(BR)G1 - G2}$	Gate to Gate Breakdown Voltage	±30	±45		V	I_G= ±1µA, I_D=I_S=0A (Open Circuit)
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	1.50		5.0	V	V_{DS} = -15V, I_D = -1nA
I_{DSS}[2]	Drain to Source Saturation Current	-2.5		-30	mA	V_{DS} = -15V, V_{GS} = 0V
I_G	Gate Operating Current		2		pA	V_{DG} = -15V, I_D = -200µA
I_{GSS}	Gate to Source Leakage Current		0.9	100	pA	V_{GS} = 15V, V_{DS} = 0V
G_{fs}	Full Conductance Transconductance	1500			µS	V_{DS} = -15V, V_{GS} = 0V, *f* = 1kHz
G_{fs}	Transconductance		1500		µS	V_{DS} = -15V, I_D = -200µA, *f* = 1kHz
G_{OS}	Full Output Conductance		38		µS	V_{DS} = -15V, V_{GS} = 0V, *f* = 1kHz
G_{OS}	Output Conductance		3		µS	V_{DS} = -15V, I_D = -200µA, *f* = 1kHz
NF	Noise Figure		0.5		db	V_{DS} = -15V, V_{GS} = 0V, R_G = 10mΩ

TYPICAL SPICE PARAMETERS FOR LSJ689 IN LT SPICE FORMAT:

```
LSJ689_4 IDSS = 14.0mA RDS=112
.MODEL  LSJ689_4 PJF  (LEVEL=1  BETA=28E-4  VTO=-2.75  LAMBDA=2E-3
+ IS=4.5E-16  N= 1  RD=73  RS=35  CGD=6E-12  CGS=11E-12  PB=0.25  MJ=0.3  FC=0.5
+ KF=2E-18  AF=1   XTI=0)
```

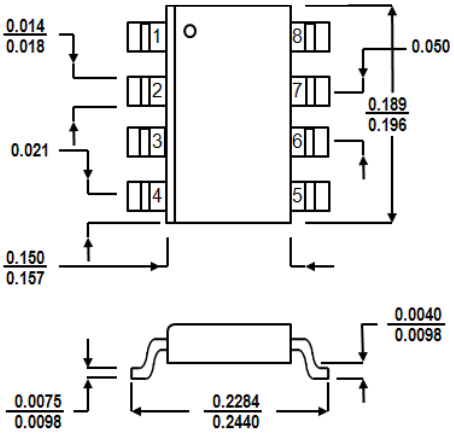
Standard Package Dimensions:

TO-71
SIX LEAD



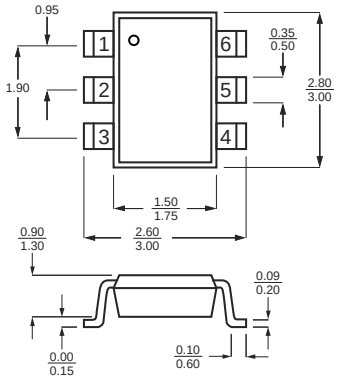
DIMENSIONS IN INCHES

SOIC-A
EIGHT LEAD



DIMENSIONS IN INCHES

SOT-23
SIX LEAD

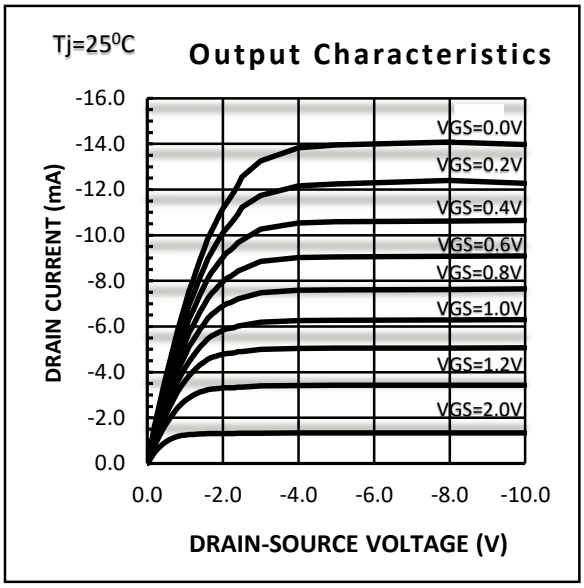


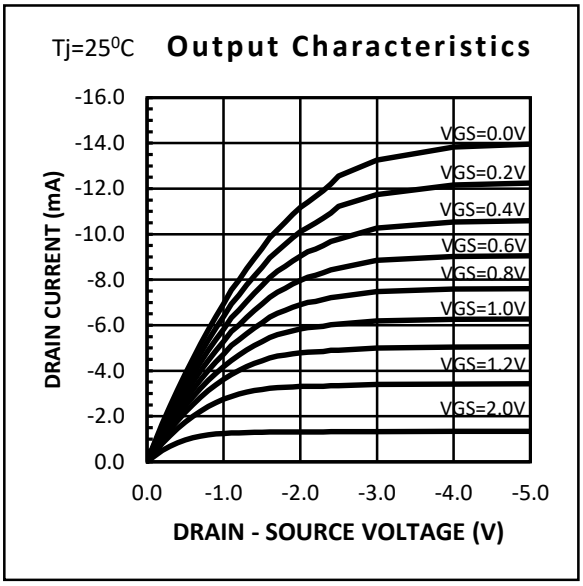
DIMENSIONS IN MILLIMETERS

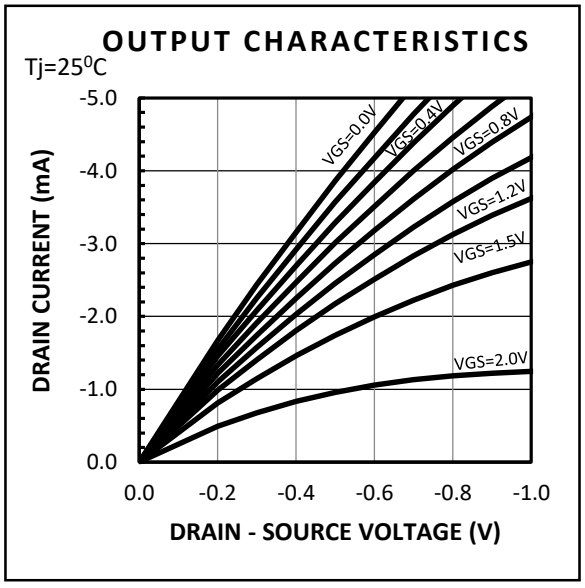
NOTES:

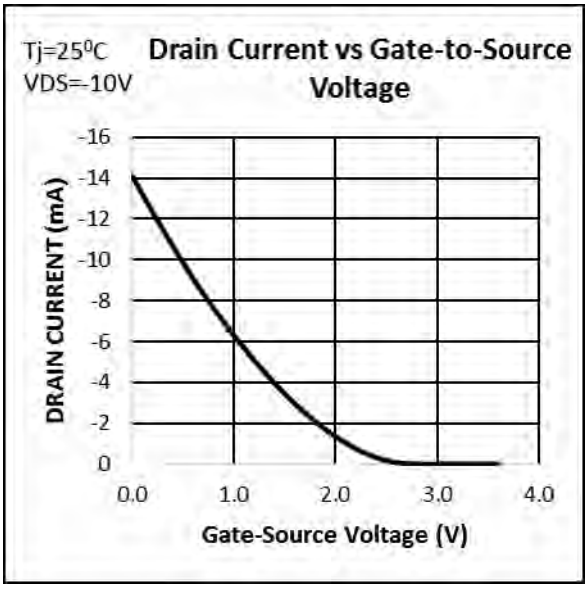
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse width ≤2$_{ms}$.
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate electrical polarity only.
4. Derate 2.4 mW/°C above 25°C.
5. Derate 4 mW/°C above 25°C.

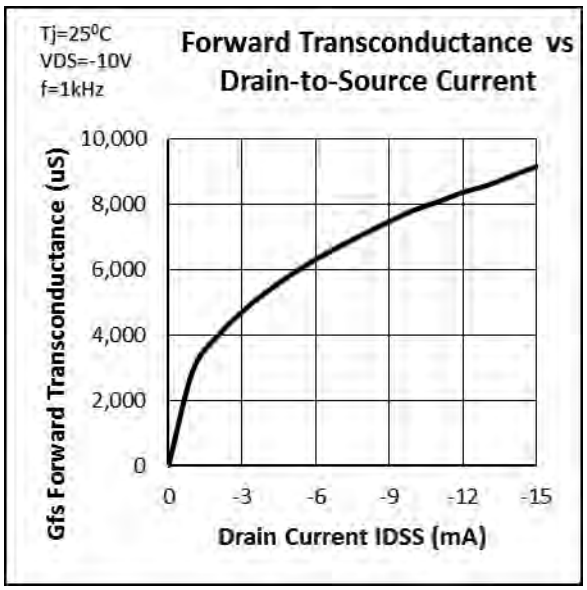
LSJ689 Typical Characteristics

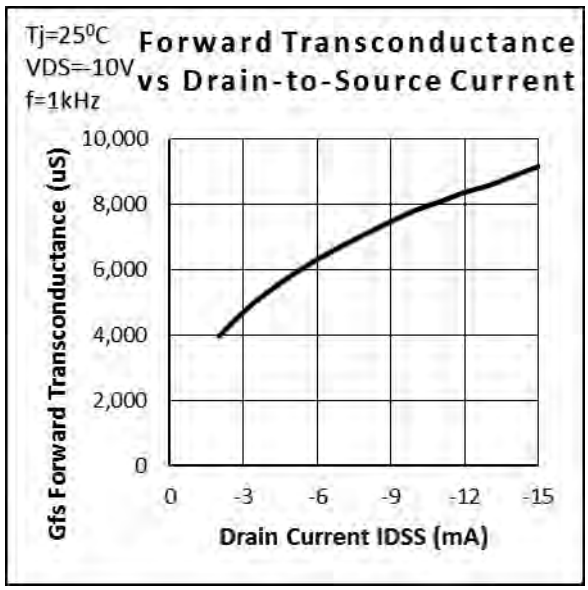




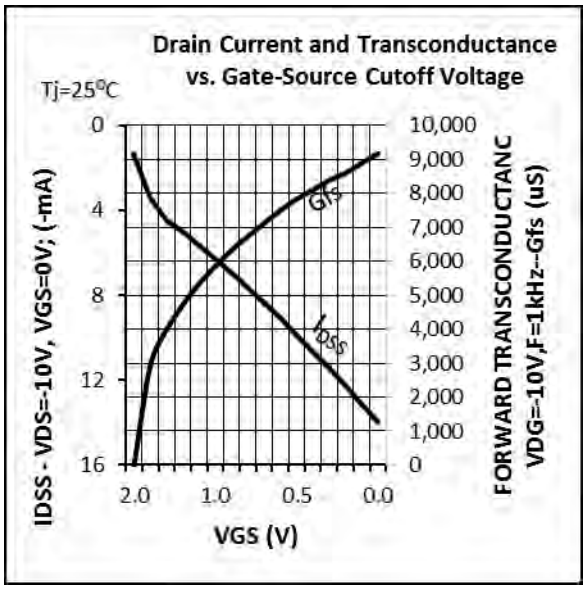


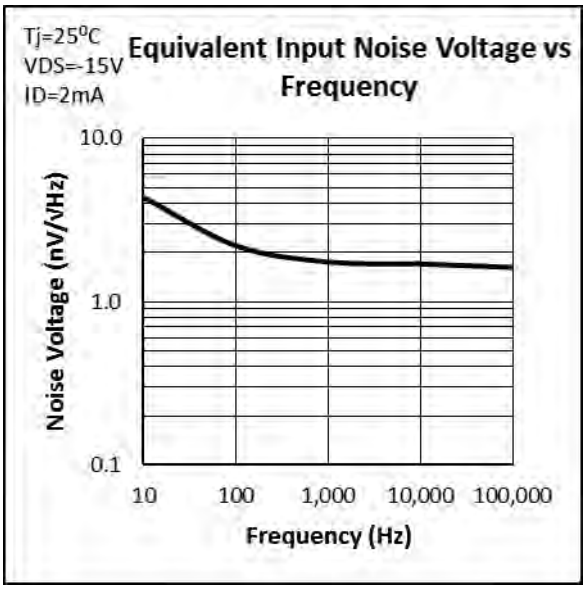


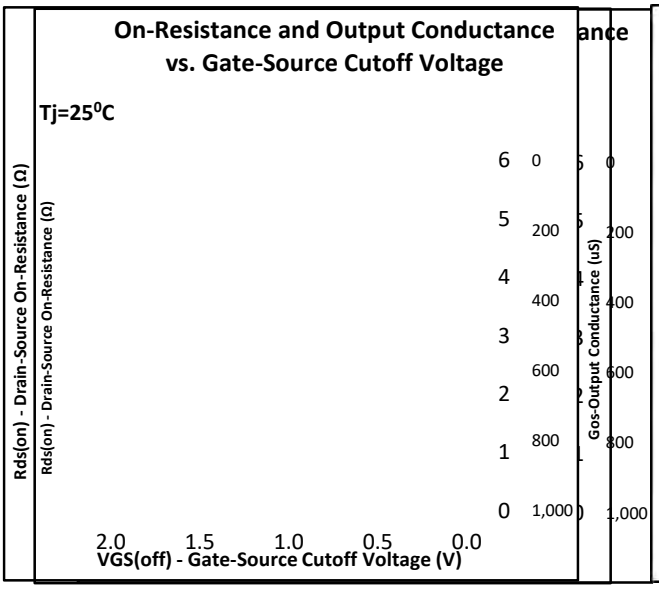


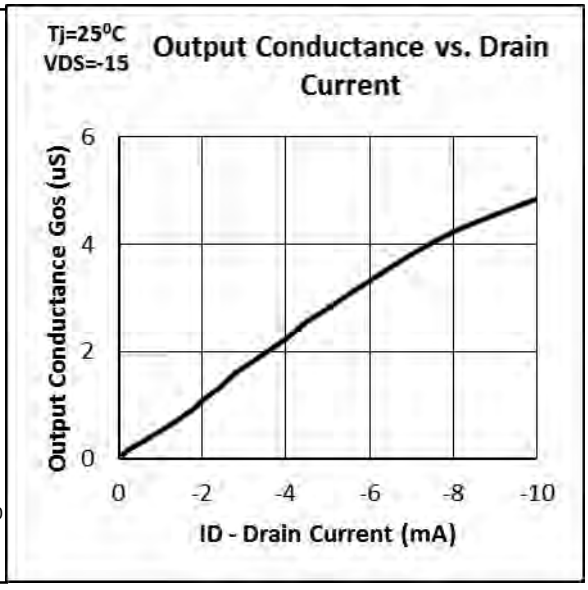


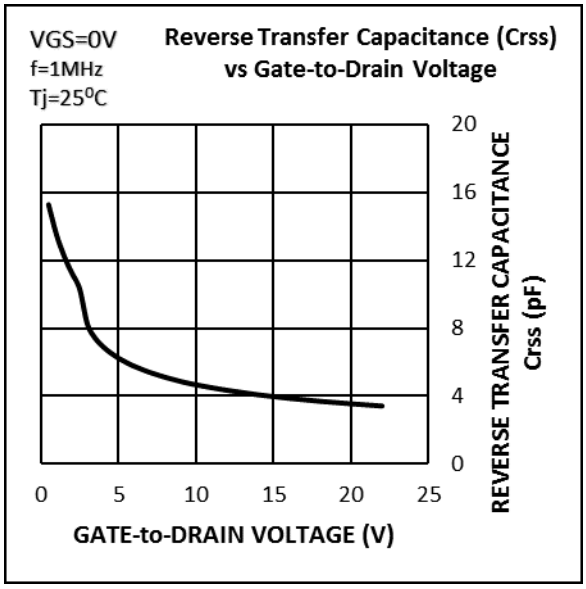
LSJ689 Typical Characteristics Continued

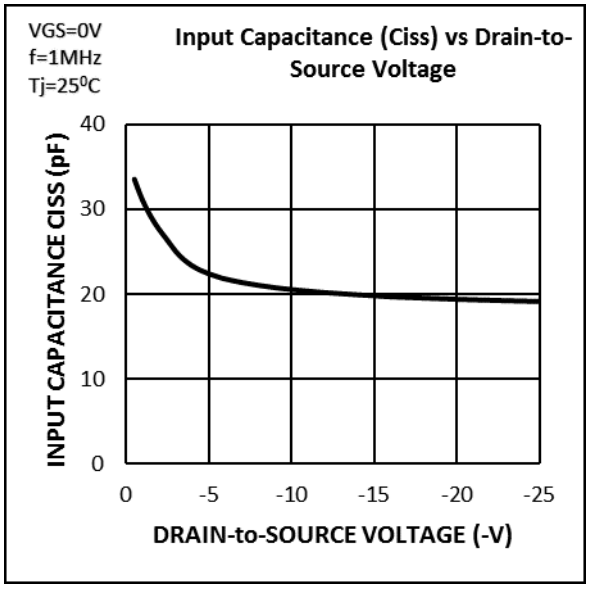




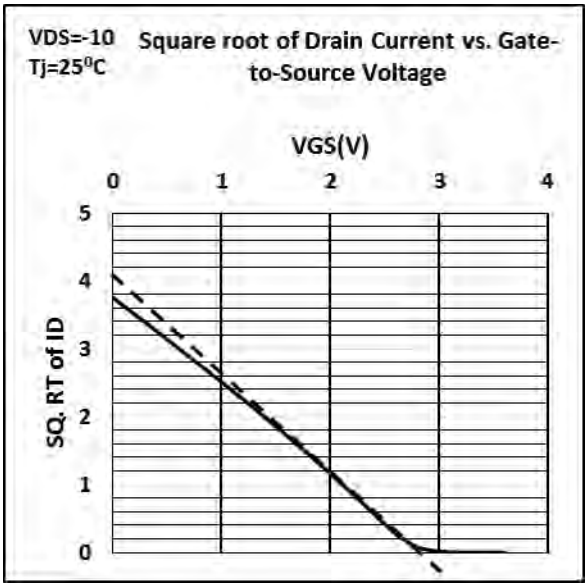








LSJ689 Typical Characteristics Continued



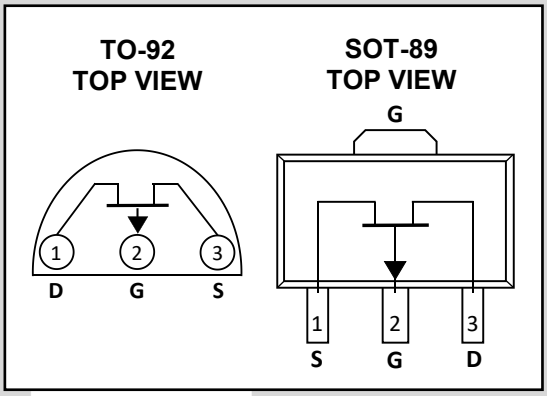
LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

LSJ74, SST74

ULTRA LOW NOISE SINGLE P-CHANNEL JFET

FEATURES	
ULTRA LOW NOISE (f = 1kHz)	e_n = 0.9nV/√Hz
HIGH GAIN	G_{fs} = 22mS (typ)
HIGH INPUT IMPEDANCE	I_G = 1.0nA
LOW CAPACITANCE	C_{RSS} = 32pF
IMPROVED SECOND SOURCE REPLACEMENT FOR 2SJ74	
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +135°C
Maximum Power Dissipation	
Continuous Power Dissipation	400mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = -10mA
Maximum Voltages	
Gate to Drain Voltage	V_{GDS} = 25V
Gate to Source Voltage	V_{GSS} = 25V

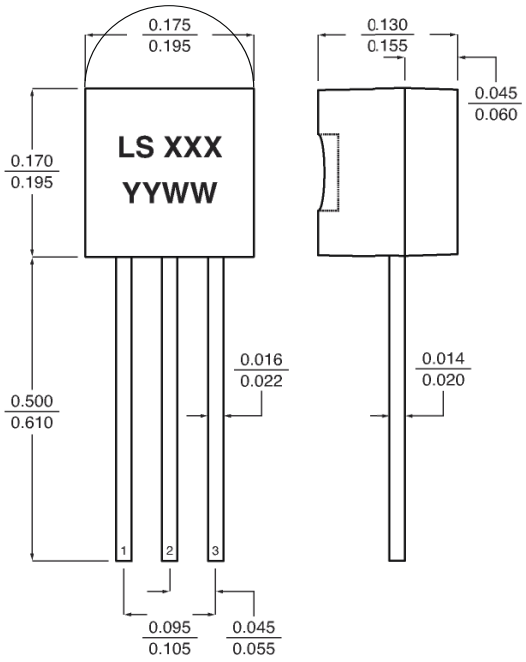


ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GDS}	Gate to Drain Breakdown Voltage		25			V	V_{DS} = 0V, I_G = 100µA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage		0.15		2		V_{DS} = -10V, I_D = -0.1µA
I_{DSS}	Drain to Source Saturation Current[2]	LSJ74A	-2.6		-6.5	mA	V_{DG} = -10V, V_{GS} = 0V
		LSJ74B	-6		-12		
		LSJ74C	-10		-20		
		LSJ74D	-17		-30		
I_G	Gate Operating Current			50		pA	V_{DG} = -10V, I_D = -1mA
I_{GSS}	Gate to Source Leakage Current				1	nA	V_{GS} = 25V, V_{DS} = 0V
G_{fss}	Full Conductance Transconductance		8	22		mS	V_{DG} = -10V, V_{GS} = 0V, f = 1kHz
e_n	Noise Voltage			1.9		nV/√Hz	V_{DS} = -10V, I_D = -2mA, f = 1kHz, NBW = 1Hz
				4			V_{DS} = -10V, I_D = -2mA, f = 10Hz, NBW = 1Hz
C_{ISS}	Common Source Input Capacitance			105		pF	V_{DS} = -10V, V_{GS} = 0V, f = 1MHz
C_{RSS}	Common Source Reverse Transfer Cap.			32			V_{DS} = -10V, I_D = 0A, f = 1MHz

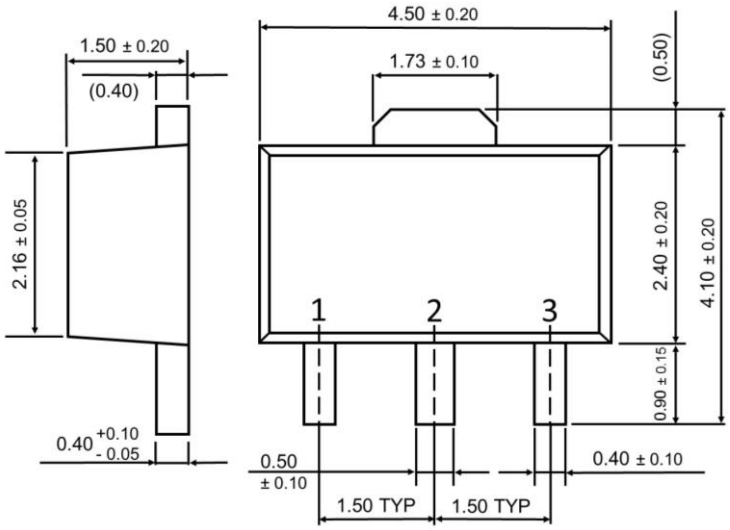
Standard Package Dimensions:

LSJ74
TO-92



Dimensions in inches

SST74
SOT-89

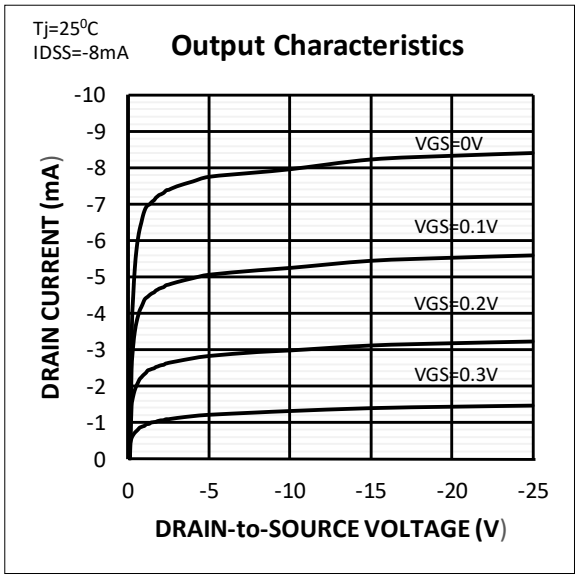


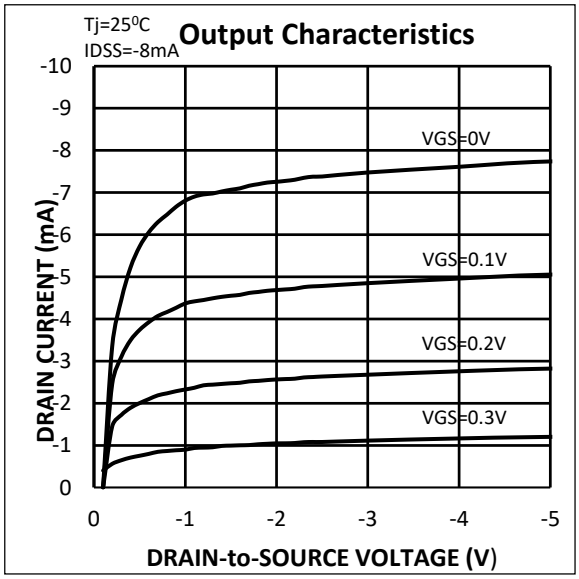
Dimensions in millimeters

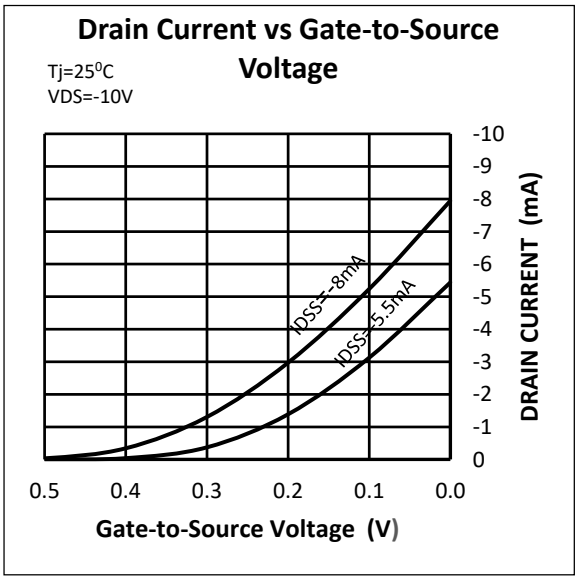
NOTES:

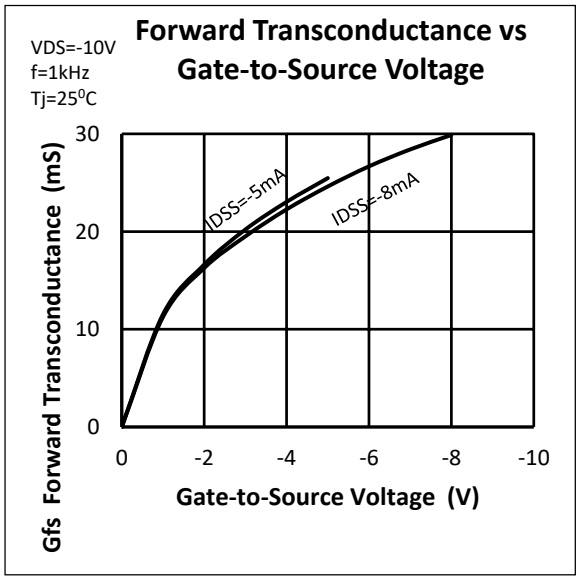
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse test: PW ≤ 300 μS, Duty Cycle ≤ 3%.
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate negative electrical polarity only.

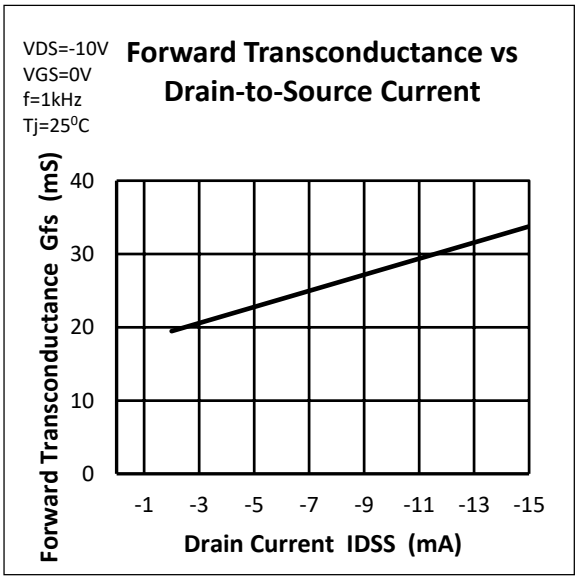
LSJ74 Typical Characteristic

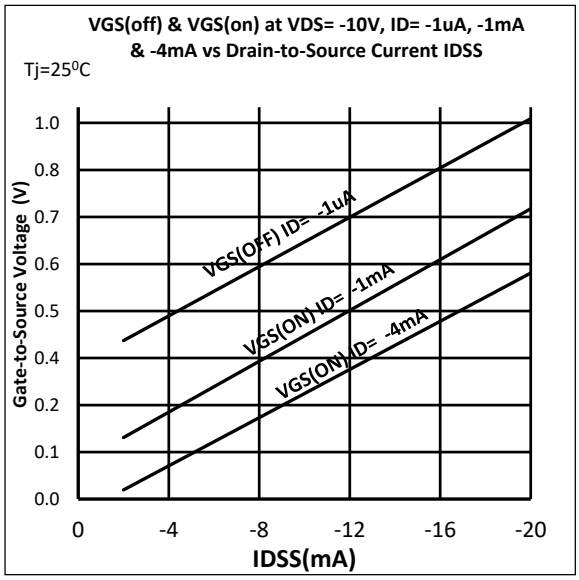




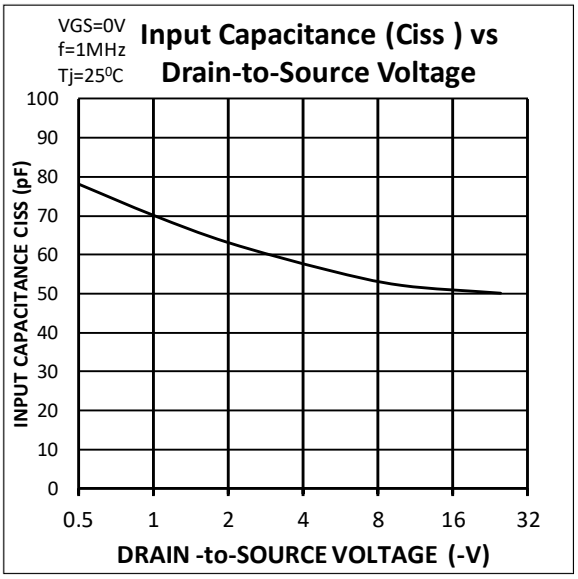


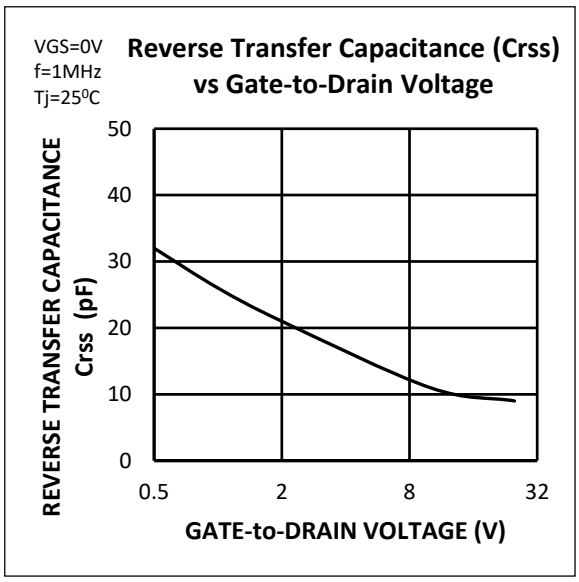


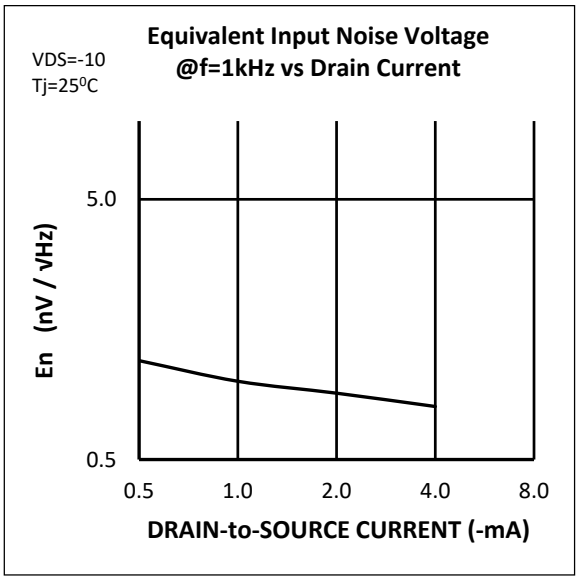


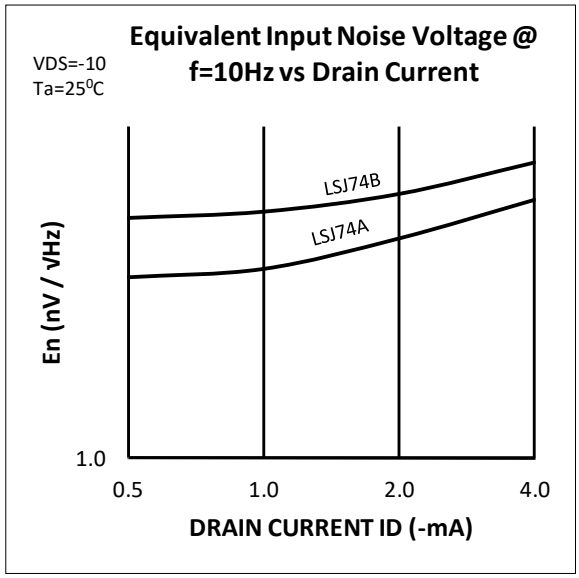


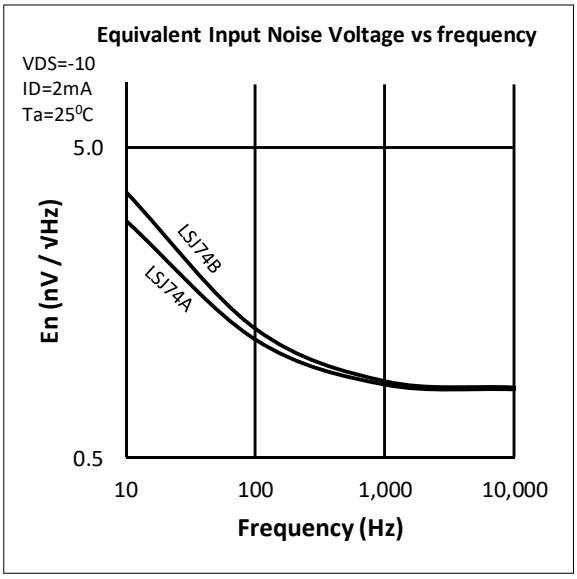
LSJ74 Typical Characteristics Continued











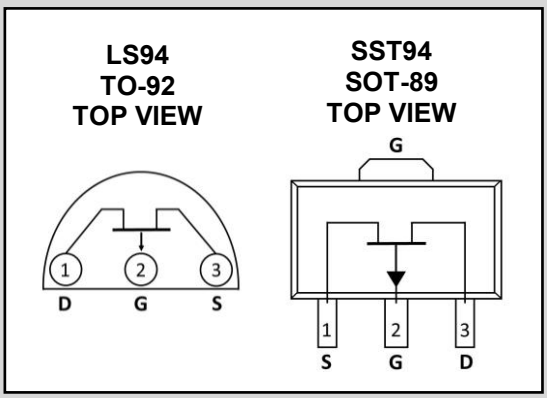
LINEAR SYSTEMS

Over Three Decades of Quality Through Innovation

LS94, SST94

GENERAL PURPOSE SINGLE P-CHANNEL JFET

FEATURES	
HIGH GAIN	G_{fs} = 22mS (typ)
HIGH INPUT IMPEDANCE	I_G = 1.0nA
LOW CAPACITANCE	C_{RSS} = 32pF
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +135°C
Maximum Power Dissipation	
Continuous Power Dissipation	400mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = -10mA
Maximum Voltages	
Gate to Drain Voltage	V_{GD} = 25V
Gate to Source Voltage	V_{GS} = 25V



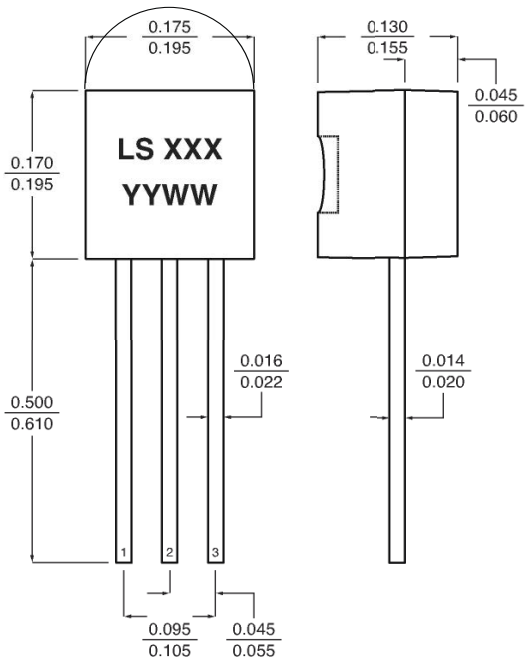
* For equivalent N-Channel, see LS190

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GDS}	Gate to Drain Breakdown Voltage	25			V	V_{DS} = 0V, I_G = 100µA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	0.15		2		V_{DS} = -10V, I_D = -0.1µA
I_{DSS}	Drain to Source Saturation Current[2]	-2.6		-30	mA	V_{DS} = -10V, V_{GS} = 0V
I_G	Gate Operating Current		50		pA	V_{DG} = -10V, I_D = -1mA
I_{GSS}	Gate to Source Leakage Current			1	nA	V_{GS} = 25V, V_{DS} = 0V
G_{fss}	Full Conductance Transconductance	8	22		mS	V_{DS} = -10V, V_{GS} = 0V, *f* = 1kHz
$R_{DS(on)}$	Drain to Source on Resistance		75	150	Ω	V_{GS} = 0V, I_D = -1mA
C_{ISS}	Common Source Input Capacitance		105		pF	V_{DS} = -10V, V_{GS} = 0V, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Cap.		32			V_{DS} = -10V, I_D = 0A, *f* = 1MHz

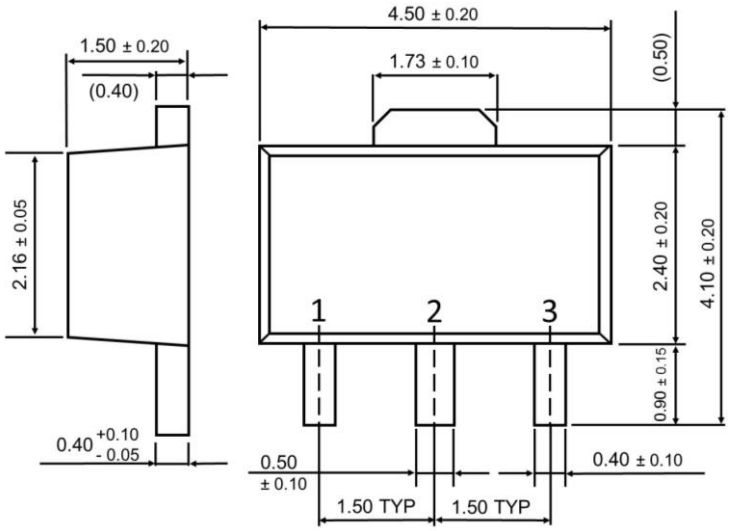
Standard Package Dimensions:

TO-92



Dimensions in inches

SOT-89



Dimensions in millimeters

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse test: PW ≤ 300 μS, Duty Cycle ≤ 3%
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate negative electrical polarity only.

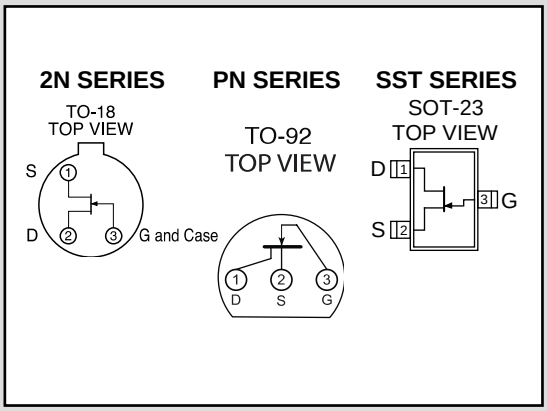
LINEAR SYSTEMS

Quality Through Innovation Since 1987

2N/PN/SST4391 SERIES

SINGLE N-CHANNEL JFET SWITCH

FEATURES	
Replacement for Siliconix 2N/PN/SST4391, 4292, & 4393	
LOW ON RESISTANCE	$r_{DS(on)} \leq 30\Omega$
FAST SWITCHING	$t_{ON} \leq 15ns$
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature (2N)	-65 to 200°C
Storage Temperature (PN/SST)	-55 to 150°C
Junction Operating Temperature (2N)	-55 to 200°C
Junction Operating Temperature (PN/SST)	-55 to 150°C
Maximum Power Dissipation	
Continuous Power Dissipation (2N)@Tc=25°C	1800mW[3]
Continuous Power Dissipation (PN/SST)	350mW[4]
Maximum Currents	
Gate Current	50mA
Maximum Voltages	
Gate to Drain or Source (2N/PN)	-40V



STATIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC		TYP	4391		4392		4393		UNIT	CONDITIONS
				MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown Voltage	2N/PN/SST		-40		-40		-40		V	I_G = -1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage	2N/PN		-4	-10	-2	-5	-0.5	-3		V_{DS} = 20V, I_D = 1nA
		SST		-4	-10	-2	-5	-0.5	-3		V_{DS} = 15V, I_D = 10nA
$V_{GS(F)}$	Gate to Source Forward Voltage		0.7		1		1		1		I_G = 1mA, V_{DS} = 0V
$V_{DS(on)}$	Drain to Source On Voltage		0.25						0.4		V_{GS} = 0V, I_D = 3mA
			0.3				0.4				V_{GS} = 0V, I_D = 6mA
			0.35		0.4						V_{GS} = 0V, I_D = 12mA
I_{DSS}	Drain to Source Saturation Current[2]	2N		50	165	25	150	5	125	mA	V_{DS} = 20V, V_{GS} = 0V
		PN		50	165	25	150	5	125		
		SST		50		25		5			
I_{GSS}	Gate Leakage Current	2N/SST	-5		-100		-100		-100	pA	V_{GS} = -20V, V_{DS} = 0V
		PN	-5		-1000		-1000		-1000		
I_G	Gate Operating Current		-5								V_{DG} = 15V, I_D = 10mA

STATIC ELECTRICAL CHARACTERISTICS CONT. @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC		TYP	4391		4392		4393		UNIT	CONDITIONS
				MIN	MAX	MIN	MAX	MIN	MAX		
$I_{D(off)}$	Drain Cutoff Current	2N	5						100	pA	V_{DS} = 20V, V_{GS} = -5V
			5				100				V_{DS} = 20V, V_{GS} = -7V
			5		100						V_{DS} = 20V, V_{GS} = -12V
		PN	5						1000		V_{DS} = 20V, V_{GS} = -5V
			5				1000				V_{DS} = 20V, V_{GS} = -7V
			5		1000						V_{DS} = 20V, V_{GS} = -12V
		SST	5		100		100		100		V_{DS} = 10V, V_{GS} = -12V
$r_{DS(on)}$	Drain to Source On Resistance				30		60		100	Ω	V_{GS} = 0V, I_D = 1mA

DYNAMIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC		TYP	4391		4392		4393		UNIT	CONDITIONS
				MIN	MAX	MIN	MAX	MIN	MAX		
g_{fs}	Forward Transconductance		6							mS	V_{DS} = 20V, I_D = 1mA *f* = 1kHz
g_{os}	Output Conductance		25							µS	
$r_{ds(on)}$	Drain to Source On Resistance				30		60		100	Ω	V_{GS} = 0V, I_D = 1mA
C_{iss}	Input Capacitance	2N	12		14		14		14	pF	V_{DS} = 20V, V_{GS} = 0V *f* = 1MHz
		PN	12		16		16		16		
		SST	13								
C_{rss}	Reverse Transfer Capacitance	2N	3.3						3.5		V_{DS} = 0V, V_{GS} = -5V *f* = 1MHz
		PN	3.5						5		
		SST	3.6								
		2N	3.2				3.5				V_{DS} = 0V, V_{GS} = -7V *f* = 1MHz
		PN	3.4				5				
		SST	3.5								
		2N	2.8		3.5						V_{DS} = 0V, V_{GS} = -12V *f* = 1MHz
		PN	3.0		5						
		SST	3.1								
e_n	Equivalent Input Noise Voltage		3							nV/√Hz	V_{DS} = 10V, I_D = 10mA *f* = 1kHz

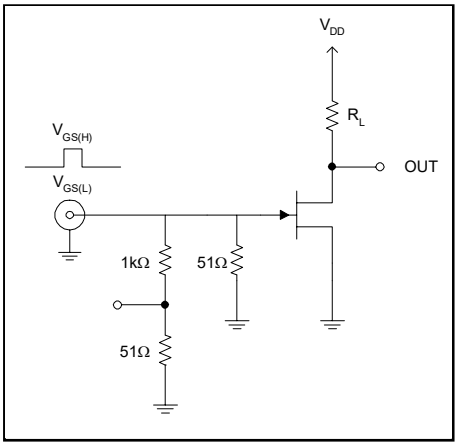
SWITCHING ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC		TYP	4391		4392		4393		UNIT	CONDITIONS
				MIN	MAX	MIN	MAX	MIN	MAX		
$t_{d(on)}$	Turn On Time	2N/PN	2		15		15		15	ns	V_{DD} = 10V, $V_{GS(H)}$ = 0V
		SST	2								
t_r		2N/PN	2		5		5		5		
		SST	2								
$t_{d(off)}$	Turn Off Time	2N/PN	6		20		35		50		
		SST	6								
t_f		2N/PN	13		15		20		30		
		SST	13								

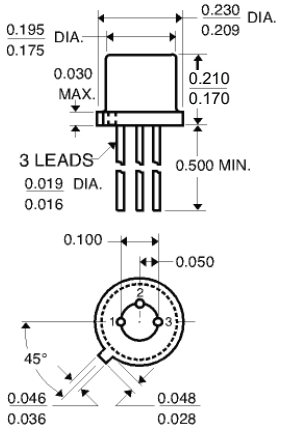
SWITCHING CIRCUIT CHARACTERISTICS

SYM.	4391	4392	4393
$V_{GS(L)}$	-12V	-7V	-5V
R_L	800Ω	1600Ω	3200Ω
$I_{D(on)}$	12mA	6mA	3mA

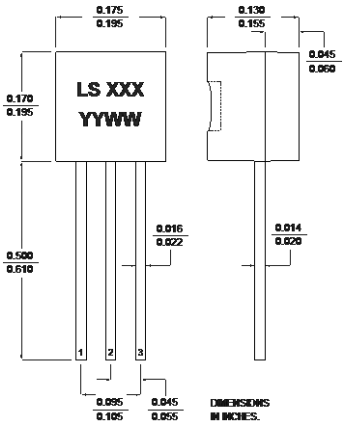
SWITCHING TEST CIRCUIT



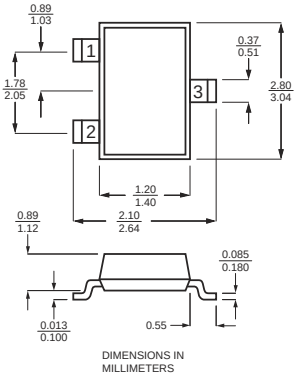
TO-18 *
Three Lead



TO-92 *



SOT-23



*Dimensions in inches

NOTES :

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse test: PW ≤ 300μs, Duty Cycle ≤ 3%
3. Derate 10mW/°C above 25°C
4. Derate 2.8mW/°C above 25°C

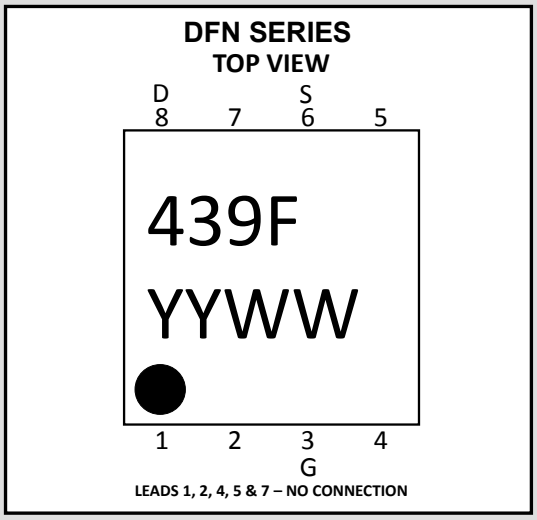
LINEAR SYSTEMS

Improved Standard Products®

4391DFN SERIES

MINIATURE/NON-MAGNETIC 8-PIN DFN PACKAGE N-CHANNEL JFET SWITCH

FEATURES	
LOW ON RESISTANCE	$r_{DS(on)} \leq 30\Omega$
FAST SWITCHING	$t_{ON} \leq 15ns$
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to 150°C
Junction Operating Temperature	-55 to 150°C
Maximum Power Dissipation	
Continuous Power Dissipation[3]	300mW
Maximum Currents	
Gate Current	50mA
Maximum Voltages	
Gate to Drain or Source	-40V



STATIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	4391DFN		4392DFN		4393DFN		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown Voltage		-40		-40		-40		V	I_G = -1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage		-4	-10	-2	-5	-0.5	-3		V_{DS} = 15V, I_D = 10nA
$V_{GS(F)}$	Gate to Source Forward Voltage	0.7		1		1		1		I_G = 1mA, V_{DS} = 0V
$V_{DS(on)}$	Drain to Source On Voltage	0.25						0.4		V_{GS} = 0V, I_D = 3mA
		0.3				0.4				V_{GS} = 0V, I_D = 6mA
		0.35		0.4						V_{GS} = 0V, I_D = 12mA
I_{DSS}	Drain to Source Saturation Current[2]		50		25		5		mA	V_{DS} = 20V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current	-.005		-1.0		-1.0		-1.0	nA	V_{GS} = -20V, V_{DS} = 0V
I_G	Gate Operating Current	-.005								V_{DG} = 15V, I_D = 10mA
$I_{D(off)}$	Drain Cutoff Current	.005		1.0		1.0		1.0	nA	V_{DS} = 10V, V_{GS} = -12V
$r_{DS(on)}$	Drain to Source On Resistance			30		60		100	Ω	V_{GS} = 0V, I_D = 1mA

DYNAMIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	4391DFN		4392DFN		4393DFN		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
g_{fs}	Forward Transconductance	6							mS	V_{DS} = 20V, I_D = 1mA
g_{os}	Output Conductance	25							µS	*f* = 1kHz
C_{iss}	Input Capacitance	13							pF	V_{DS} = 20V, V_{GS} = 0V *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance	3.6								V_{DS} = 0V, V_{GS} = -5V *f* = 1MHz
		3.5								V_{DS} = 0V, V_{GS} = -7V *f* = 1MHz
		3.1								V_{DS} = 0V, V_{GS} = -12V *f* = 1MHz
e_n	Equivalent Input Noise Voltage	3							nV/√Hz	V_{DS} = 10V, I_D = 10mA *f* = 1kHz

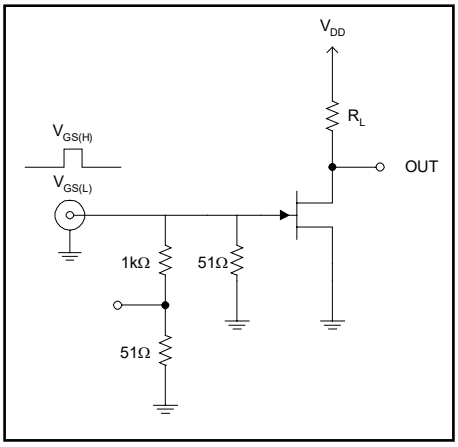
SWITCHING ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	4391DFN		4392DFN		4393DFN		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
$t_{d(on)}$	Turn On Time	2							ns	V_{DD} = 10V, $V_{GS(H)}$ = 0V
t_r		2								
$t_{d(off)}$	Turn Off Time	6								
t_f		13								

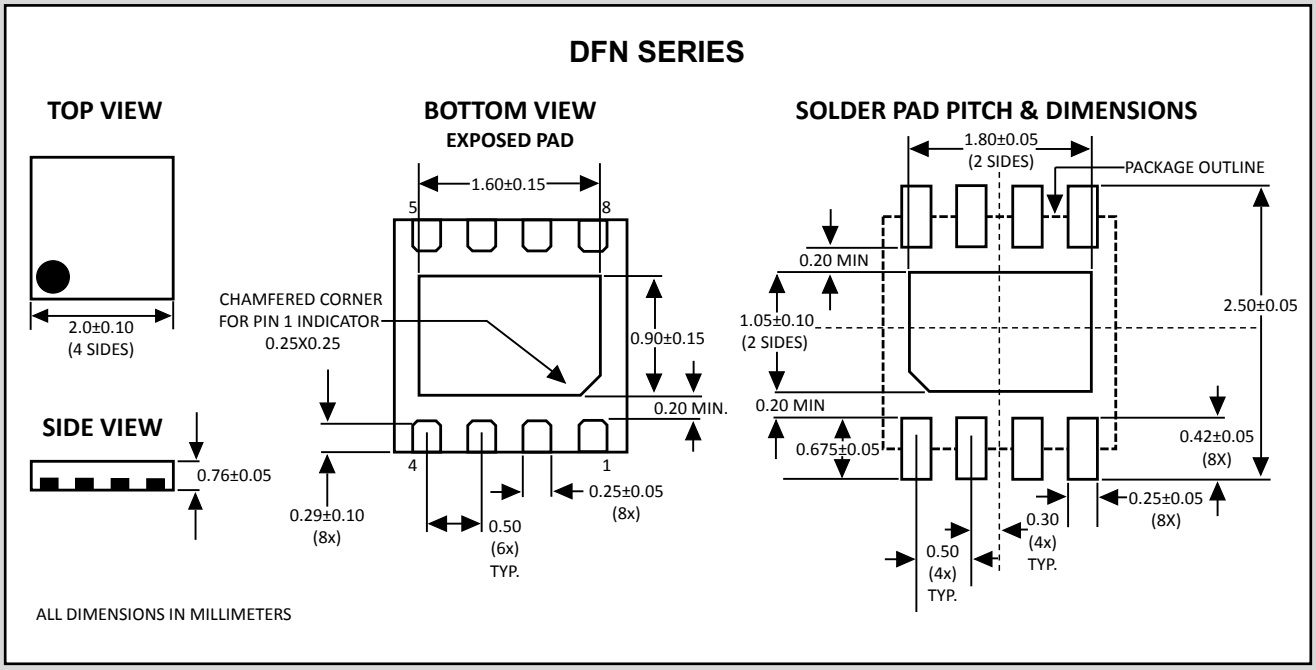
SWITCHING CIRCUIT CHARACTERISTICS

SYM.	4391DFN	4392DFN	4393DFN
$V_{GS(L)}$	-12V	-7V	-5V
R_L	800Ω	1600Ω	3200Ω
$I_{D(on)}$	12mA	6mA	3mA

SWITCHING TEST CIRCUIT



Standard Package Dimensions:



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse test: PW ≤ 300μs, Duty Cycle ≤ 3%
3. Derate 2.8mW/°C above 25°C

LINEAR SYSTEMS

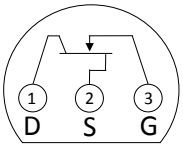
Improved Standard Products®

J/SST111 SERIES

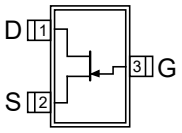
SINGLE N-CHANNEL JFET SWITCH

FEATURES	
DIRECT REPLACEMENT FOR SILICONIX J/SST111 SERIES	
LOW GATE LEAKAGE CURRENT	5pA
FAST SWITCHING	4ns
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to 150°C
Junction Operating Temperature	-55 to 150°C
Maximum Power Dissipation	
Continuous Power Dissipation (J)[3]	360mW
Continuous Power Dissipation (SST)[3]	350mW
Maximum Currents	
Gate Current	50mA
Maximum Voltages	
Gate to Drain	-35V
Gate to Source	-35V

J SERIES
TO-92
TOP VIEW



SST SERIES
SOT-23
TOP VIEW



STATIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	J/SST111		J/SST112		J/SST113		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown Voltage		-35		-35		-35		V	I_G = -1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage		-3	-10	-1	-5		-3		V_{DS} = 5V, I_D = 1µA
$V_{GS(F)}$	Gate to Source Forward Voltage	0.7								I_G = 1mA, V_{DS} = 0V
I_{DSS}	Drain to Source Saturation Current[2]		20		5		2		mA	V_{DS} = 15V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current	-0.005		-1		-1		-1	nA	V_{GS} = -15V, V_{DS} = 0V
I_G	Gate Operating Current	-5							pA	V_{DG} = 15V, I_D = 1.0mA
$I_{D(off)}$	Drain Cutoff Current	0.005		1		1		1	nA	V_{DS} = 5V, V_{GS} = -10V
$r_{DS(on)}$	Drain to Source On Resistance			30		50		100	Ω	V_{GS} = 0V, V_{DS} = 0.1V

DYNAMIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	J/SST111		J/SST112		J/SST113		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
g_{fs}	Forward Transconductance	6							mS	V_{DS} = 20V, I_D = 1mA
g_{os}	Output Conductance	25							µS	*f* = 1kHz
$r_{ds(on)}$	Drain to Source On Resistance			30		50		100	Ω	V_{GS} = 0V, I_D = 1mA *f* = 1kHz
C_{iss}	Input Capacitance	7		12		12		12	pF	V_{DS} = 0V, V_{GS} = -10V
C_{rss}	Reverse Transfer Capacitance	3		5		5		5		*f* = 1MHz
e_n	Equivalent Noise Voltage	3							nV/√Hz	V_{DG} = 10V, I_D = 1mA *f* = 1 kHz

SWITCHING CHARACTERISTICS

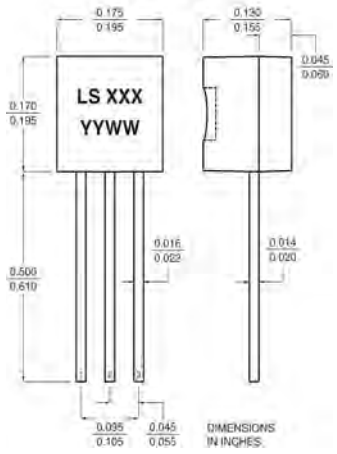
SYM.	CHARACTERISTIC	TYP	UNIT	CONDITIONS
$t_{d(on)}$	Turn On Time	2	ns	V_{DD} = 10V $V_{GS(H)}$ = 0V
t_r		2		
$t_{d(off)}$	Turn Off Time	6		
t_f		15		

SWITCHING CIRCUIT CHARACTERISTICS

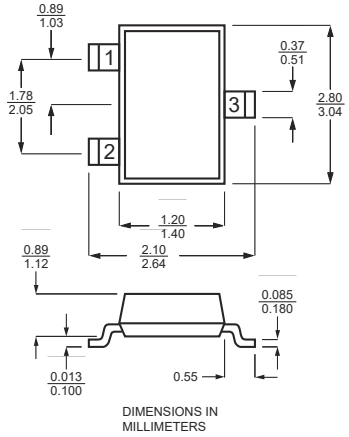
SYM.	J/SST111	J/SST112	J/SST113
$V_{GS(L)}$	-12V	-7V	-5V
R_L	800Ω	1600Ω	3200Ω
$I_{D(on)}$	12mA	6mA	3mA

STANDARD PACKAGE DIMENSIONS:

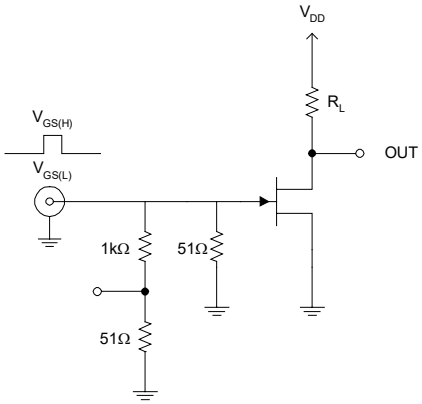
TO-92



SOT-23



SWITCHING TEST CIRCUIT



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. Derate 2.8mW/°C above 25°C

LINEAR SYSTEMS

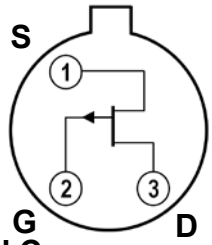
Improved Standard Products®

2N5018 SERIES

SINGLE P-CHANNEL JFET SWITCH

FEATURES	
DIRECT REPLACEMENT FOR SILICONIX 2N5018	
ZERO OFFSET VOLTAGE	
LOW ON RESISTANCE	75Ω
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to 150°C
Junction Operating Temperature	-55 to 150°C
Maximum Power Dissipation	
Continuous Power Dissipation[3]	500mW
Maximum Currents	
Gate Current	-10mA
Maximum Voltages	
Gate to Drain	30V
Gate to Source	30V

TO-18
TOP VIEW



STATIC ELECTRICAL CHARACERISTICS @25ºC (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	2N5018		2N5019		UNITS	CONDITIONS
			MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown Voltage		30		30		V	I_G = 1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage			10		5		V_{DS} = -15V, I_D = -1µA
$V_{DS(on)}$	Drain to Source On Voltage			-0.5				V_{GS} = 0V, I_D = -6mA
						-0.5		V_{GS} = 0V, I_D = -3mA
I_{DSS}	Drain to Source Saturation Current[2]		-10		-5		mA	V_{DS} = -20V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current			2		2	nA	V_{GS} = 15V, V_{DS} = 0V
$I_{D(off)}$	Drain Cutoff Current			-10		-10		V_{DS} = -15V, V_{GS} = 12V
						-10	µA	V_{DS} = -15V, V_{GS} = 7V
I_{DGO}	Drain Reverse Current			-2		-2	nA	V_{DG} = -15V, I_S = 0A
$r_{DS(on)}$	Drain to Source On Resistance			75		150	Ω	I_D = -1mA, V_{GS} = 0V

DYNAMIC ELECTRICAL CHARACTERISTICS @25ºC (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	2N5018		2N5019		UNITS	CONDITIONS
			MIN	MAX	MIN	MAX		
$r_{ds(on)}$	Drain to Source On Resistance			75		150	Ω	I_D = -100μA, V_{GS} = 0V *f* = 1kHz
C_{iss}	Input Capacitance			45		45	pF	V_{DS} = -15V, V_{GS} = 0V *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance			10				V_{DS} = 0V, V_{GS} = 12V *f* = 1MHz
						10		V_{DS} = 0V, V_{GS} = 7V *f* = 1MHz

SWITCHING CHARACTERISTICS (max)

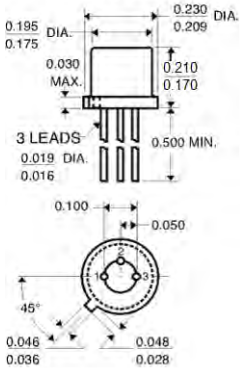
SYM.	CHARACTERISTIC	2N5018	2N5019	UNITS
$t_{d(on)}$	Turn On Time	15	15	ns
t_r		20	75	
$t_{d(off)}$	Turn Off Time	15	25	
t_f		50	100	

SWITCHING CIRCUIT CHARACTERISTICS

SYM.	2N5018	2N5019
V_{DD}	-6V	-6V
V_{GG}	12V	8V
R_L	910Ω	1.8KΩ
R_G	220Ω	390Ω
$I_{D(on)}$	-6mA	-3mA
$V_{GS(H)}$	0V	0V
$V_{GS(L)}$	12V	7V

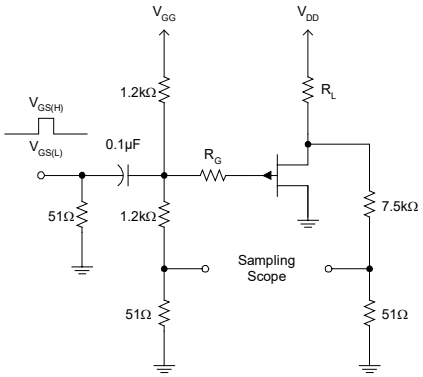
STANDARD PACKAGE DIMENSIONS:

TO-18
Three Lead



Note: All Dimensions in inches

SWITCHING TEST CIRCUIT



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse test: PW ≤ 300μs, Duty Cycle ≤ 3%
3. Derate 3mW/°C above 25°C.

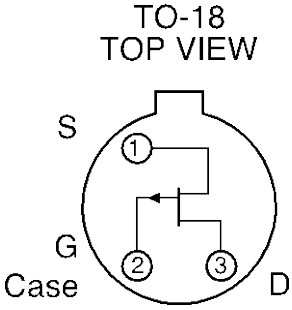
LINEAR SYSTEMS

Improved Standard Products®

2N5114 SERIES

SINGLE P-CHANNEL JFET SWITCH

FEATURES	
REPLACEMENT FOR SILICONIX 2N5114, 2N5115, 2N5116	
LOW ON RESISTANCE	75Ω
LOW CAPACITANCE	6pF
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to 150°C
Junction Operating Temperature	-55 to 150°C
Maximum Power Dissipation	
Continuous Power Dissipation[3]	500mW
Maximum Currents	
Gate Current	-50mA
Maximum Voltages	
Gate to Drain	30V
Gate to Source	30V



STATIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	2N5114		2N5115		2N5116		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown Voltage		30		30		30		V	I_G = 1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage		5	10	3	6	1	4		V_{DS} = -15V, I_D = -1nA
$V_{GS(F)}$	Gate to Source Forward Voltage	-0.7		-1		-1		-1		I_G = -1mA, V_{DS} = 0V
$V_{DS(on)}$	Drain to Source On Voltage	-1.0		-1.3						V_{GS} = 0V, I_D = -15mA
		-0.7				-0.8				V_{GS} = 0V, I_D = -7mA
		-0.5						-0.6		V_{GS} = 0V, I_D = -3mA
I_{DSS}	Drain to Source Saturation Current[2]		-30	-195					mA	V_{DS} = -18V, V_{GS} = 0V
					-15	-110	-5	-55		V_{DS} = -15V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current	5		500		500		500	pA	V_{GS} = 20V, V_{DS} = 0V
I_G	Gate Operating Current	-5								V_{DG} = -15V, I_D = -1mA
$I_{D(off)}$	Drain Cutoff Current	-10		-500						V_{DS} = -15V, V_{GS} = 12V
		-10				-500				V_{DS} = -15V, V_{GS} = 7V
		-10						-500		V_{DS} = -15V, V_{GS} = 5V
$r_{DS(on)}$	Drain to Source On Resistance			75		100		150	Ω	V_{GS} = 0V, I_D = -1mA

Note: All Min & Max limits are absolute values. Negative signs indicate electrical polarity only.

DYNAMIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	2N5114		2N5115		2N5116		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
g_{fs}	Forward Transconductance	4.5							mS	V_{DS} = -15V, I_D = -1mA *f* = 1kHz
g_{os}	Output Conductance	20							µS	
$r_{ds(on)}$	Drain to Source On Resistance			75		100		150	Ω	V_{GS} = 0V, I_D = -1mA *f* = 1kHz
C_{iss}	Input Capacitance	20		25		25		25	pF	V_{DS} = -15V, V_{GS} = 0V *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance	5		7						V_{DS} = 0V, V_{GS} = 12V *f* = 1MHz
		6				7				V_{DS} = 0V, V_{GS} = 7V *f* = 1MHz
		6						7		V_{DS} = 0V, V_{GS} = 5V *f* = 1MHz
e_n	Equivalent Noise Voltage	20							nV/√Hz	V_{DG} = -10V, I_D = -10mA *f* = 1 kHz

SWITCHING CHARACTERISTICS (max)

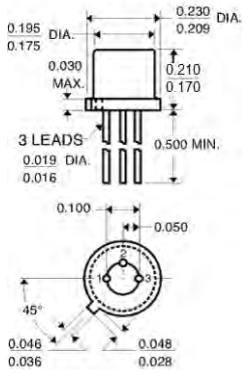
SYM.	CHARACTERISTIC	2N5114	2N5115	2N5116	UNITS
$t_{d(on)}$	Turn On Time	6	10	12	ns
t_r		10	20	30	
$t_{d(off)}$	Turn Off Time	6	8	10	
t_f		15	30	50	

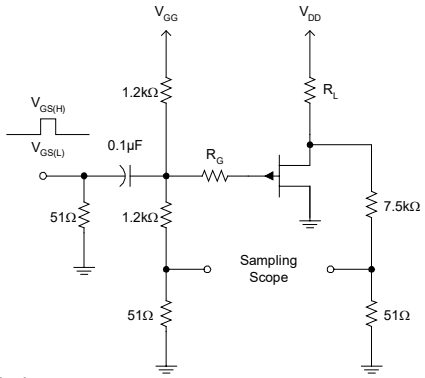
SWITCHING CIRCUIT CHARACTERISTICS

SYM.	2N5114	2N5115	2N5116
V_{DD}	-10V	-6V	-6V
V_{GG}	20V	12V	8V
R_L	430Ω	910Ω	2kΩ
R_G	100Ω	220Ω	390Ω
$I_{D(on)}$	-15mA	-7mA	-3mA
$V_{GS(H)}$	0V	0V	0V
$V_{GS(L)}$	-11V	-7V	-5V

STADARD PACKAGE DIMENSIONS:

TO-18
Three Lead





Note: All Dimensions are in inches

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. Derate 3mW/°C above 25°C.

LINEAR SYSTEMS

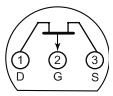
Over 30 Years of Quality Through Innovation

J/SST174 SERIES

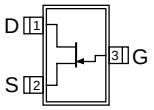
SINGLE P-CHANNEL JFET SWITCH

FEATURES	
Replacement For SILICONIX J/SST174 SERIES	
LOW ON RESISTANCE	$r_{DS(on)} \leq 85\Omega$
LOW GATE OPERATING CURRENT	$I_{D(off)}$ = 10pA
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to 150°C
Junction Operating Temperature	-55 to 135°C
Maximum Power Dissipation	
Continuous Power Dissipation[3]	350mW
Maximum Currents	
Gate Current	I_G = -50mA
Maximum Voltages	
Gate to Drain Voltage	V_{GDS} = 30V
Gate to Source Voltage	V_{GSS} = 30V

J SERIES
TO-92
TOP VIEW



SST SERIES
SOT-23
TOP VIEW



COMMON ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	30			V	I_G = 1µA, V_{DS} = 0V
$V_{GS(F)}$	Gate to Source Forward Voltage		-0.7			I_G = -1mA, V_{DS} = 0V
I_{GSS}	Gate Reverse Current		0.01	1	nA	V_{GS} = 20V, V_{DS} = 0V
I_G	Gate Operating Current		0.01			V_{DG} = -15V, I_D = -1mA
$I_{D(off)}$	Drain Cutoff Current		-0.01	-1		V_{DS} = -15V, V_{GS} = 10V

SPECIFIC ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	J/SST174		J/SST175		J/SST176		J/SST177		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$V_{GS(off)}$	Gate to Source Cutoff Voltage	5	10	3	6	1	4	0.8	2.25	V	V_{DS} = -15V, I_D = -10nA
I_{DSS}	Drain to Source Saturation Current	-20	-195	-7	-90	-2	-55	-1.5	-30	mA	V_{DS} = -15V, V_{GS} = 0V
$r_{DS(on)}$	Drain to Source On Resistance		85		125		250		300	Ω	V_{GS} = 0V, V_{DS} = -0.1V

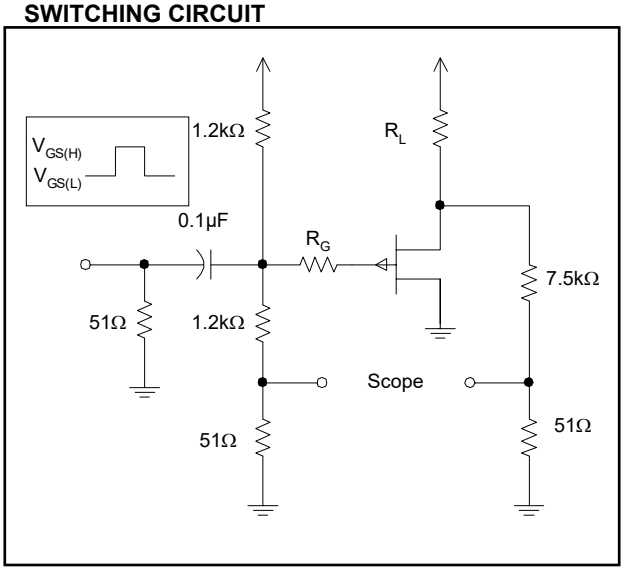
SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	TYP	UNITS	CONDITIONS
$t_{d(on)}$	Turn On Time	10	ns	$V_{GS(L)}$ = 0V $V_{GS(H)}$ = 10V See Switching Circuit
t_r	Turn On Rise Time	15		
$t_{d(off)}$	Turn Off Time	10		
t_f	Turn Off Fall Time	20		

SWITCHING CIRCUIT PARAMETERS

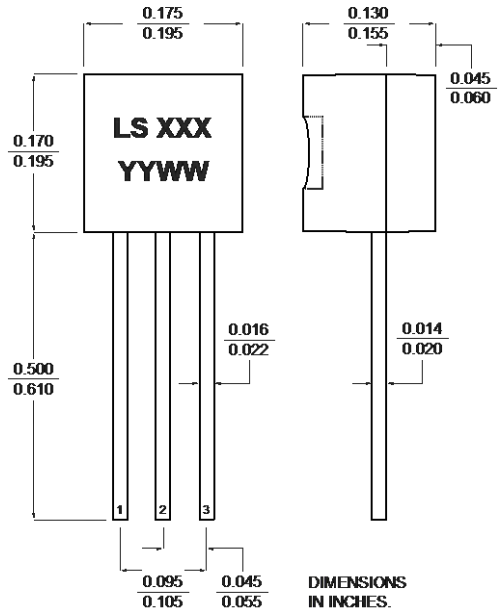
	J/SST174	J/SST175	J/SST176	J/SST177
V_{DD}	-10V	-6V	-6V	-6V
V_{GG}	20V	12V	8V	5V
R_L	560Ω	750Ω	1800Ω	5600Ω
R_G	100Ω	220Ω	390Ω	390Ω
$I_{D(on)}$	-15mA	-7mA	-3mA	-1mA

SWITCHING CIRCUIT

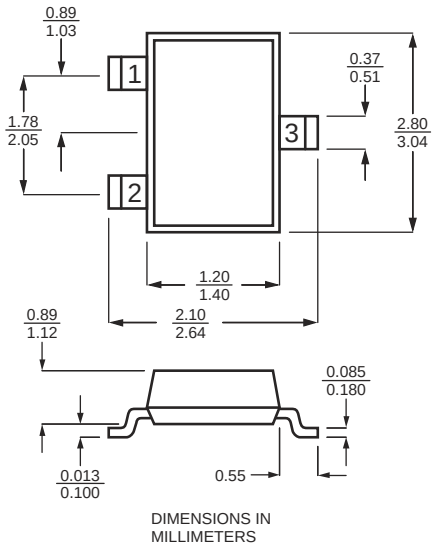


STANDARD PACKAGE DIMENSIONS:

TO-92



SOT-23



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulsed test: $P_W \leq 300\mu S$ Duty Cycle: 3%
3. Derate 2.8mW/°C above 25 °C.

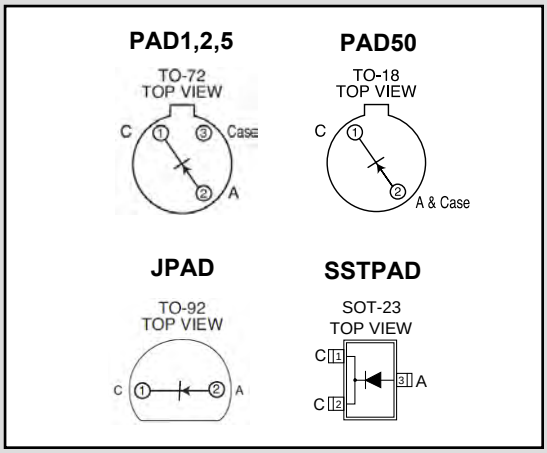
LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

PAD SERIES

PICO AMPERE DIODES

FEATURES	
DIRECT REPLACEMENT FOR SILICONIX PAD SERIES	
REVERSE BREAKDOWN VOLTAGE	$BV_R \geq -30V$
REVERSE CAPACITANCE	$C_{rss} \leq 2.0pF$
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Maximum Power Dissipation	
Continuous Power Dissipation (PAD)	300mW
Continuous Power Dissipation (J/SSTPAD)	350mW
Maximum Currents	
Forward Current (PAD)	50mA
Forward Current (J/SSTPAD)	10mA



COMMON ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_R	Reverse Breakdown Voltage	ALL PAD	-45			V	I_R = -1µA
		ALL SSTPAD	-30				
		ALL JPAD	-35				
V_F	Forward Voltage			0.8	1.5		I_F = 5mA
C_{rss}	Total Reverse Capacitance	PAD1,5		0.5	0.8	pF	V_R = -5V, *f* = 1MHz
		All Others		1.5	2		

SPECIFIC ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		PAD	JPAD	SSTPAD	UNITS	CONDITIONS
I_R	Maximum Reverse Leakage Current	PAD1	-1			pA	V_R = -20V
		PAD2	-2				
		(SST/J)PAD5	-5	-5	-5		
		(SST/J)PAD10	-10	-10	-10		
		(SST/J)PAD20	-20	-20	-20		
		(SST/J)PAD50	-50	-50	-50		
		(SST/J)PAD100	-100	-100			
		(SST/J)PAD200		-200			
		(SST/J)PAD500		-500			

1. Derate 2mW/°C above 25°C
2. Derate 2.8mW/°C above 25°C

Figure 1. Operational Amplifier Protection
Input Differential Voltage limited to 0.8V (typ) by JPADs D_1 and D_2. Common Mode Input voltage limited by JPADs D_3 and D_4 to ±15V.

Figure 2. Sample and Hold Circuit
Typical Sample and Hold circuit with clipping. JPAD diodes reduce offset voltages fed capacitively from the JFET switch gate.

FIGURE 1

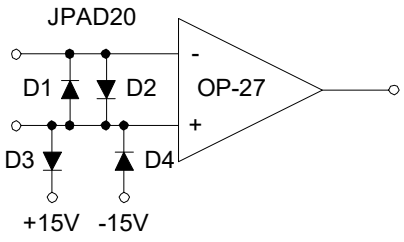
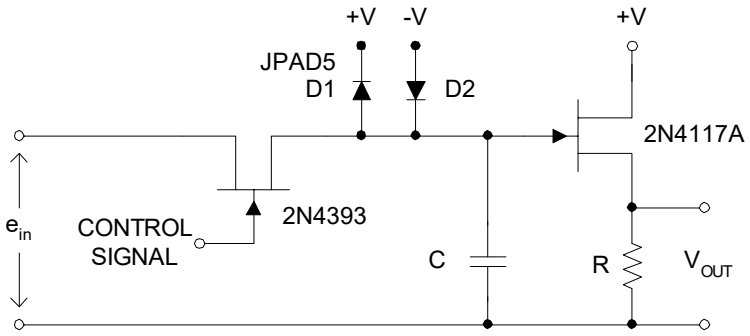
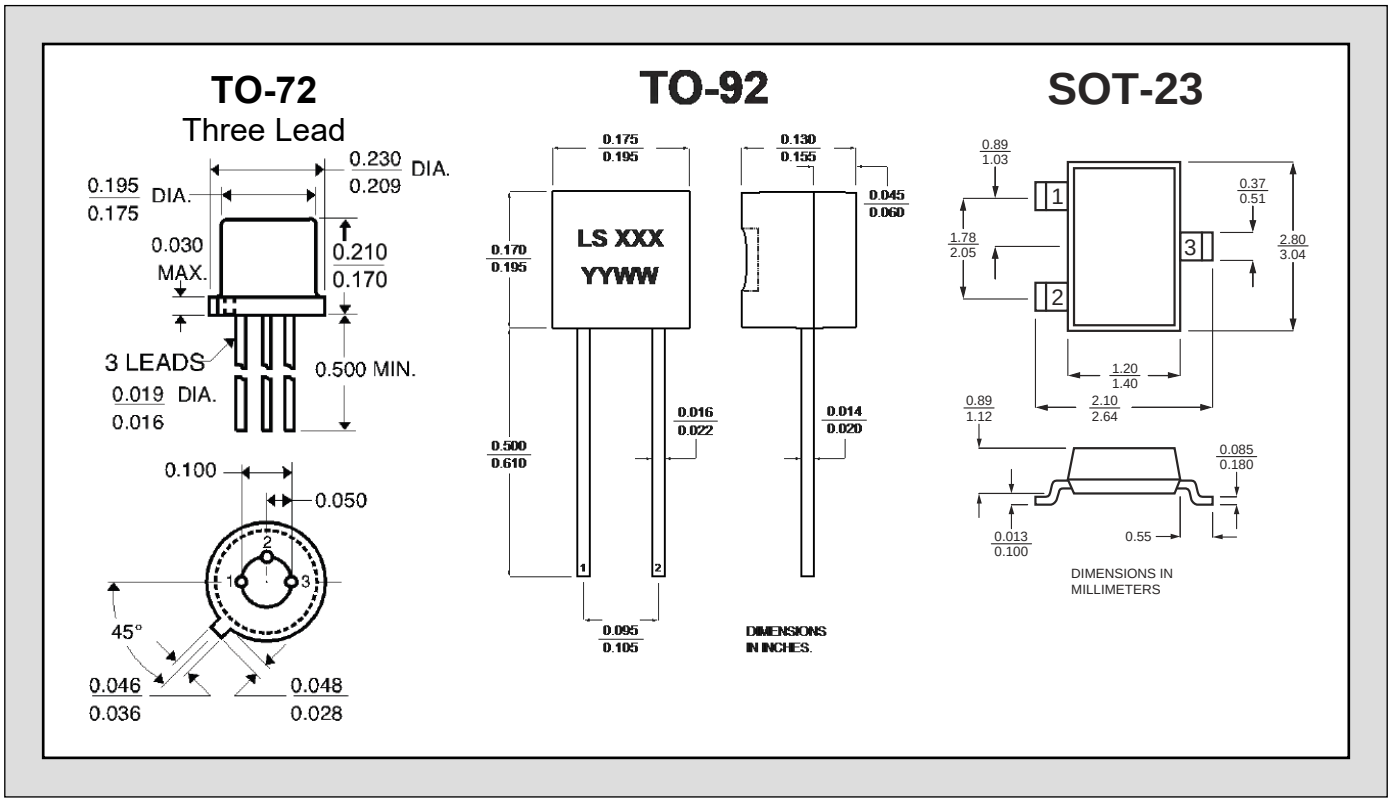


FIGURE 2





NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. The PAD type number denotes its maximum reverse current value in pico amperes. Devices with I_R values intermediate to those shown are available upon request.

LINEAR SYSTEMS

Improved Standard Products®

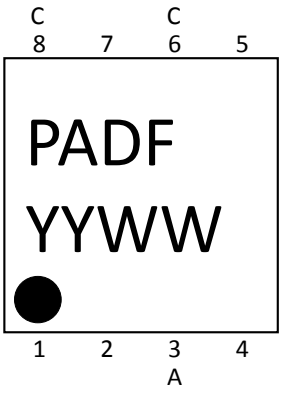
PAD-DFN SERIES

MINIATURE/NON MAGNETIC 8-PIN DFN PACKAGE LOW LEAKAGE DIODE

FEATURES	
REVERSE BREAKDOWN VOLTAGE	$BV_R \geq -30V$
REVERSE CAPACITANCE	$C_{rss} \leq 2.0pF$
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Maximum Power Dissipation[2]	
Continuous Power Dissipation	300mW
Maximum Currents	
Forward Current	10mA

DFN SERIES

TOP VIEW



LEADS 1, 2, 4, 5 & 7 – NO CONNECTION

COMMON ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_R	Reverse Breakdown Voltage	-30			V	I_R = -1µA
V_F	Forward Voltage		0.8	1.5		I_F = 5mA
C_{rss}	Total Reverse Capacitance		1.5		pF	V_R = -5V, *f* = 1MHz

SPECIFIC ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		TYP	UNITS	CONDITIONS
I_R	Maximum Reverse Leakage Current	PAD5DFN	-5	pA	V_R = -20V
		PAD50DFN	-50		

Figure 1. Operational Amplifier Protection
Input Differential Voltage limited to 0.8V (typ) by DFNs D_1 and D_2. Common Mode Input voltage limited by DFNs D_3 and D_4 to ±15V.

Figure 2. Sample and Hold Circuit
Typical Sample and Hold circuit with clipping. DFN diodes reduce offset voltages fed capacitively from the JFET switch gate.

FIGURE 1

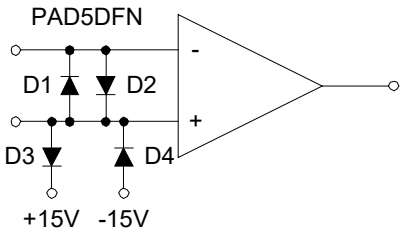
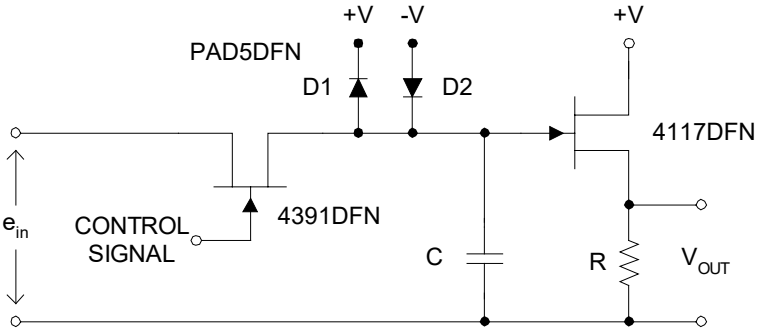
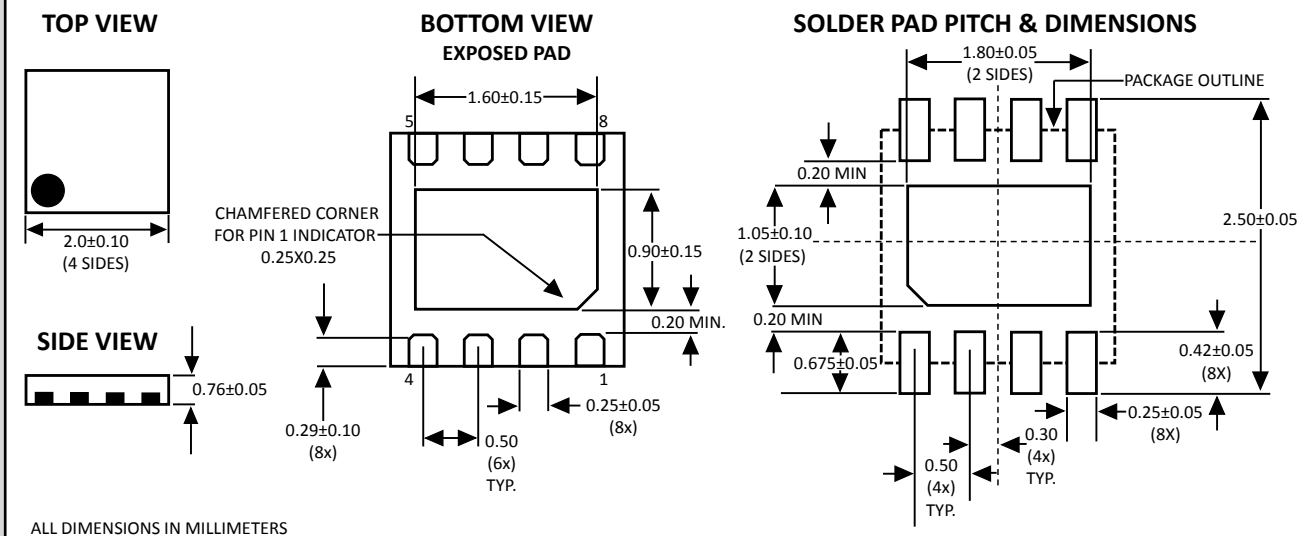


FIGURE 2



DFN PACKAGE



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Derate 2.8 mW/ºC above 25ºC
3. The PAD type number denotes its maximum reverse current value in pico amperes. Devices with I_R values intermediate to those shown are available upon request.

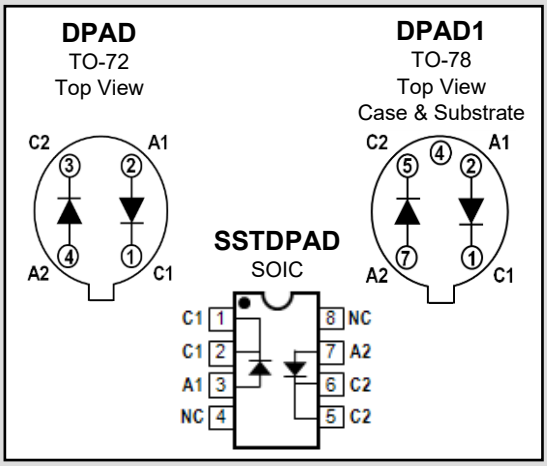
LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

DPAD SERIES

MONOLITHIC DUAL PICO AMPERE DIODES

FEATURES	
Direct Replacement For SILICONIX DPAD SERIES	
HIGH ON ISOLATION	20fA
EXCELLENT CAPACITANCE MATCHING	$\Delta C_R \leq 0.2pF$
ABSOLUTE MAXIMUM RATINGS[1] @ 25°C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55ºC to +150°C
Operating Junction Temperature	-55ºC to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation (DPAD)[3]	500mW
Maximum Currents	
Forward Current (DPAD)	50mA



* Case and Pin 4 must be floating on all TO-78 case devices

COMMON ELECTRICAL CHARACTERISTICS @ 25ºC (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_R	Reverse Breakdown Voltage	DPAD1	-45			V	I_R= -1µA
		DPAD2,5,10,20,50,100	-45				
		SSTDPAD5,50,100	-30				
V_F	Forward Voltage			0.8	1.5		I_F= 1mA
$\lvert C_{R1} - C_{R2} \rvert$	Differential Capacitance (ΔC_R)	DPAD1			0.2	pF	$V_{R1} = V_{R2}$ = -5V, *f*=1MHz
		ALL OTHERS			0.5		
C_{rss}	Total Reverse Capacitance	DPAD1			0.8		V_R = -5V, *f*=1MHz
		DPAD2,5,10,20,50,100			2.0		
		SSTDPAD5,50,100			4.0		

SPECIFIC ELECTRICAL CHARACTERISTICS @ 25ºC (unless otherwise stated)

SYMBOL	CHARACTERISTIC		DPAD[2]	SSTDPAD[2]	UNITS	CONDITIONS
I_R	Maximum Reverse Leakage Current[2]	(SST)DPAD1	-1		pA	V_R = -20V
		(SST)DPAD2	-2			
		(SST)DPAD5	-5	-5		
		(SST)DPAD10	-10			
		(SST)DPAD20	-20			
		(SST)DPAD50	-50	-50		
		(SST)DPAD100	-100	-100		

Figure 1. Operational Amplifier Protection
Input Differential Voltage limited to 0.8V (typ) by DPADs D_1 and D_2. Common Mode Input voltage limited by DPADs D_3 and D_4 to ±15V.

Figure 2. Sample and Hold Circuit
Typical Sample and Hold circuit with clipping. DPAD diodes reduce offset voltages fed capacitively from the JFET switch gate.

FIGURE 1

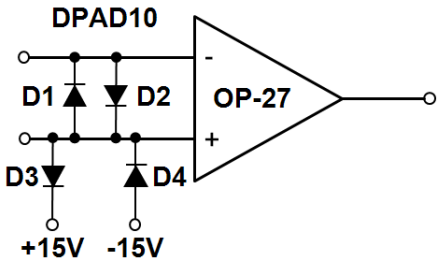
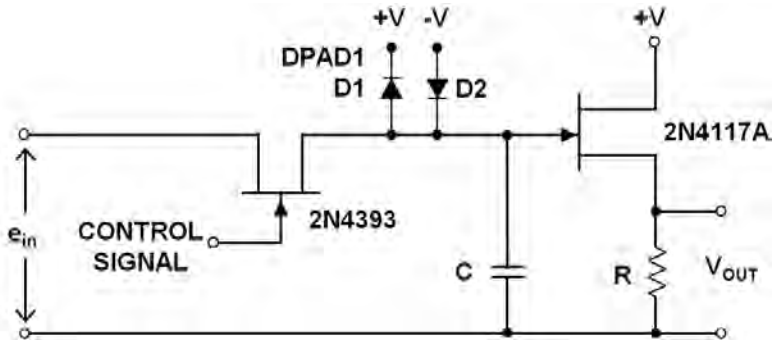
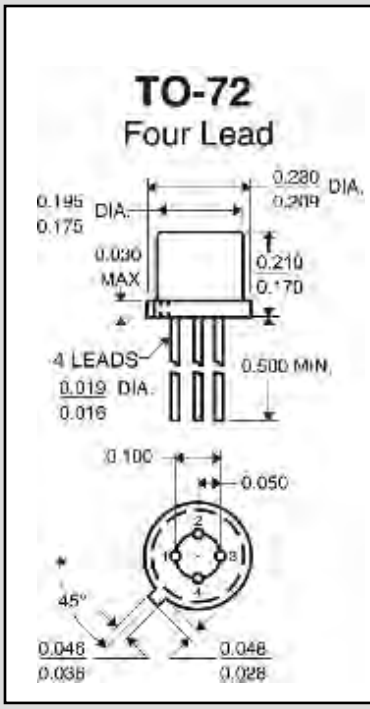
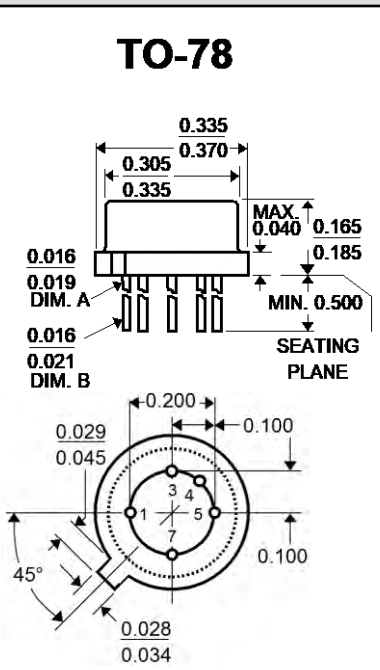
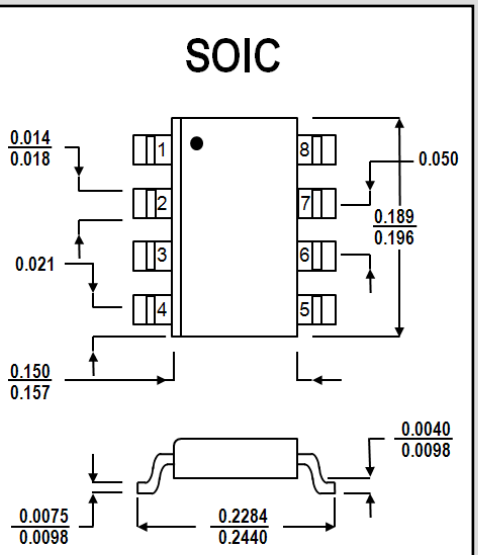


FIGURE 2









NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. The DPAD type number denotes its maximum reverse current value in pico amperes. Devices with I_R values intermediate to those shown are available upon request.
3. Derate 4 mW/ºC above 25ºC

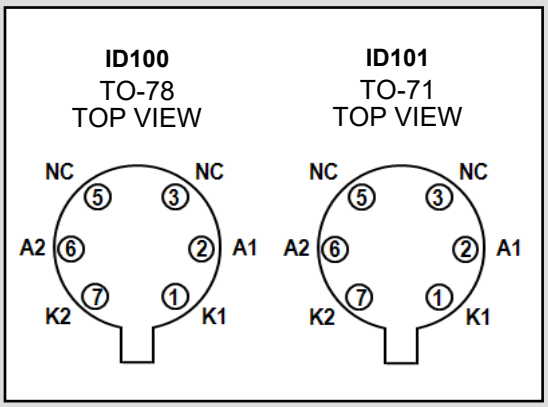
LINEAR SYSTEMS

Improved Standard Products®

ID100 ID101

MONOLITHIC DUAL PICO AMPERE DIODES

FEATURES	
DIRECT REPLACEMENT FOR INTERSIL ID100 & ID101	
REVERSE LEAKAGE CURRENT	I_R = 0.1pA
REVERSE BREAKDOWN VOLTAGE	$BV_R \geq$ 30V
REVERSE CAPACITANCE	C_{rss} = 0.75pF
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Maximum Power Dissipation @ TA = + 25°	
Continuous Power Dissipation	300mW
Maximum Currents	
Forward Current	20mA
Reverse Current	100µA
Maximum Voltages	
Reverse Voltage	30V
Diode to Diode Voltage	±50V



ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_R	Reverse Breakdown Voltage	30			V	I_R = 1µA
V_F	Forward Voltage	0.8		1.1		I_F = 10mA
I_R	Reverse Leakage Current		0.1		pA	V_R = 1V
			2.0	10		V_R = 10V
$\|I_{R1}-I_{R2}\|$	Differential Leakage Current			3		
C_{rss}	Total Reverse Capacitance[2]		0.75	1	pF	V_R = 10V, *f* = 1MHz

Figure 1. Operational Amplifier Protection
Input Differential Voltage limited to 0.8V (typ) by Diodes ID100 D_1 and D_2.
Common Mode Input voltage limited by Diodes ID100 D_3 and D_4 to ±15V.

Figure 2. Sample and Hold Circuit
Typical Sample and Hold circuit with clipping. ID100 diodes reduce offset voltages fed capacitively from the ID100 switch gate.

FIGURE 1

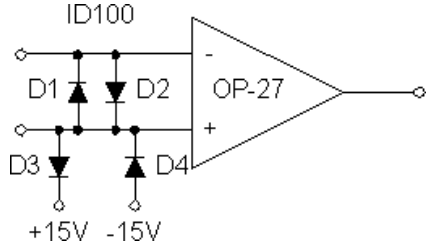
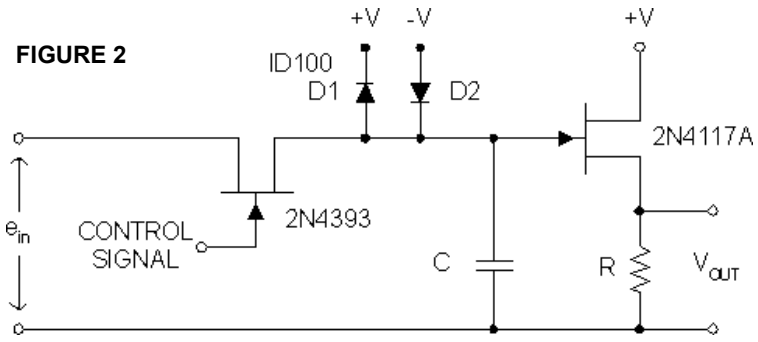
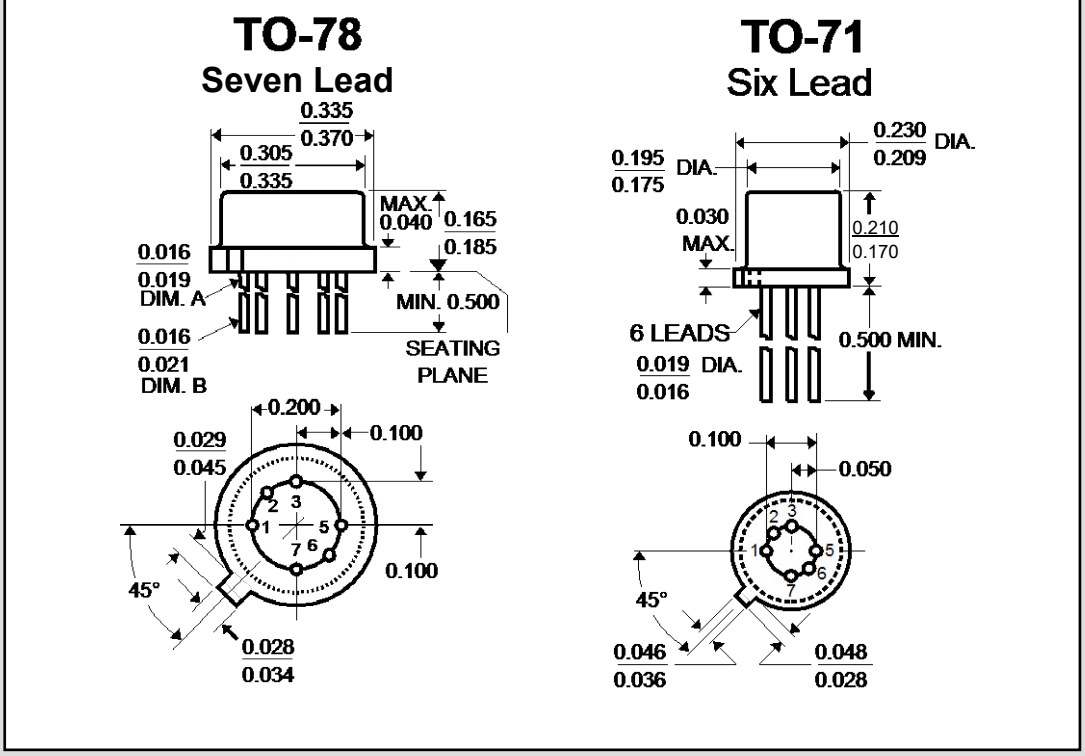


FIGURE 2



STANDARD PACKAGE DIMENSIONS:



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Design reference only, not 100% tested.
3. Pins 3 & 5 on ID100 and ID101 must not be connected, in any fashion or manner, to any circuit or node.

LINEAR SYSTEMS

Improved Standard Products®

SD-SST210/214

N-CHANNEL LATERAL DMOS SWITCH

PART NUMBER	$V_{(BR)DS}$ Min (V)	$V_{(GS)th}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD210DE	30	1.5	45 @ V_{GS}=10V	0.5	2
SD214DE	20	1.5	45 @ V_{GS}=10V	0.5	2
SST210	30	1.5	50 @ V_{GS}=10V	0.5	2
SST214	20	1.5	50 @ V_{GS}=10V	0.5	2

PRODUCT SUMMARY

Features

- Ultra-High Speed Switching—t_{ON}: 1ns
- Ultra-Low Reverse Capacitance: 0.2pF
- Low Guaranteed r_{DS} @5V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

Benefits

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

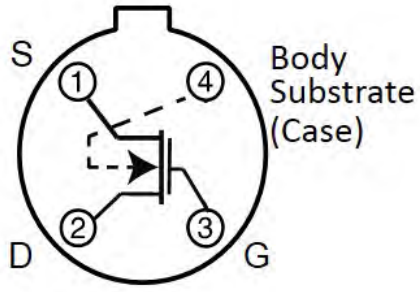
Description

The SD210DE/214 and SST210/214 are enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video and high-frequency applications. The SD214DE and SST214 are normally used for ±10-V analog switching. These MOSFETs utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. These MOSFETs do not have a gate protection Zener diode which results in lower gate leakage and ± voltage capability from gate to substrate. A poly-silicon gate is featured for manufacturing reliability.

For similar products see: quad array—SD5000/5400 series, Zener protected—SD211DE/SST211 Series.

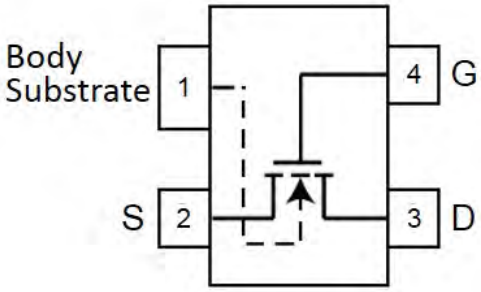
Top Views

SD210DE, SD214DE



TO-206AF
(TO-72)

SST210, SST214



TO-253
(SOT-143)

Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Gate-Drain, Gate-Source Voltage . . . . . ± 40V
Gate-Substrate Voltage . . . . . ± 30V
Drain-Source Voltage (SD210DE/SST210) 30V
(SD214DE/SST214) 20V
Source-Drain Voltage (SD210DE/SST210) 10V
(SD214DE/SST214) 20V
Drain-Substrate Voltage (SD210DESST210) 30V
(SD214DE/SST214) 25V

Source-Substrate Voltage (SD210DE/SST210) 15V
(SD210DE/SST210) 25V
Drain Current 50mA
Lead Temperature (1/16" from ease for 10 seconds) . . . . . 300°C
Storage Temperature . . . . . -65 to 150°C
Operating Junction Temperature . . . . . -55 to 125°C
Power Dissipation* 300mW

Note:
* Derate 3mW/°C above 25°C

Specifications[a]

PARAMETER	SYMBOL	TEST CONDITIONS		TYP	LIMITS 210 Series Min	LIMITS 210 Series Max	LIMITS 214 Series Min	LIMITS 214 Series Max	UNIT
Static									
Drain - Source Breakdown Voltage	$V_{(BR)DS}$	V_{GS} = V_{BS} = 0V, I_D = 10 µA		35	30				V
		V_{GS} = V_{BS} = -5V, I_D = 10 nA		30	10		20		
Source - Drain Breakdown Voltage	$V_{(BR)SD}$	V_{GD} = V_{BD} = -5V, I_S = 10 nA		22	10		20		
Drain - Substrate Breakdown Voltage	$V_{(BR)DBO}$	V_{GB} = 0V, I_D= 10 nA Source Open		35	15		25		
Source - Substrate Breakdown Voltage	$V_{(BR)SBO}$	V_{GB} = 0V, I_s = 10 µA Drain Open		35	15		25		
Drain – Source Leakage	$I_{DS(off)}$	V_{GS} = V_{BS} = -5V	V_{DS} = 10V	0.4		10			nA
			V_{DS} = 20V	0.9				10	
Source - Drain Leakage	$I_{SD(off)}$	V_{GD} = V_{BD} = -5V	V_{SD} = 10V	0.5		10			
			V_{SD} = 20V					10	
Gate Leakage	I_{GBS}	V_{DB} = V_{SB} = 0V, V_{GB} = ±40V		±0.001		±100		±100	pA
Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 µA , V_{SB} = 0V		0.8	0.5	1.5	0.1	1.5	V
Drain – Source On-Resistance	$r_{DS(on)}$	V_{SB} = 0V I_D = 1mA	V_{GS} = 5V (SD Series)	58		70		70	Ω
			V_{GS} = 5V (SST Series)	60		75		75	
			V_{GS} = 10V (SD Series)	38		45		45	
			V_{GS} = 10V (SST Series)	40		50		50	
			V_{GS} = 15V	30					
			V_{GS} = 20V	26					
			V_{GS} = 25V	24					

Specifications[a]

PARAMETER	SYMBOL[b]	TEST CONDITIONS[b]		TYP[c]	LIMITS				UNIT
					210 Series		214 Series		
					Min	Max	Min	Max	
Dynamic									
Forward Transconductance	g_{fs}	V_{DS} = 10V, V_{SB} = 0V, I_D = 20mA, f = 1kHz	SD Series	11	10		10		mS
			SST Series	10.5	9		9		
	g_{os}		All	0.9					
Gate Node Capacitance	$C_{(GS+GD+GB)}$	V_{DS} = 10V, f = 1MHz V_{GS} = V_{BS} = -15V	SD Series	2.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5	
Reverse Transfer Capacitance	C_{rss}		SST Series	4.2					
			SD Series	0.2		0.5		0.5	
Switching									
Turn-On Time	$t_{D(on)}$	SD Series Only V_{SB} = 0V, V_{IN} 0 to 5V, R_G = 25Ω V_{DD} = 5V, R_L = 680Ω		0.5		1		1	ns
	t_r			0.6		1		1	
Turn-Off Time	$t_{D(off)}$			2					
	t_f			6					

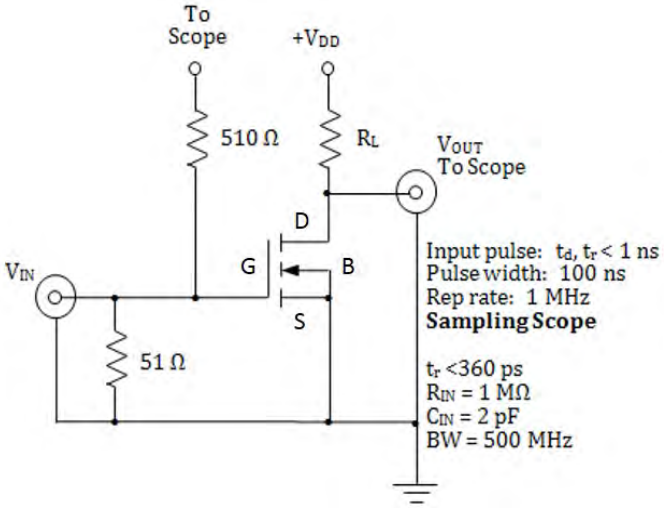
NOTES:

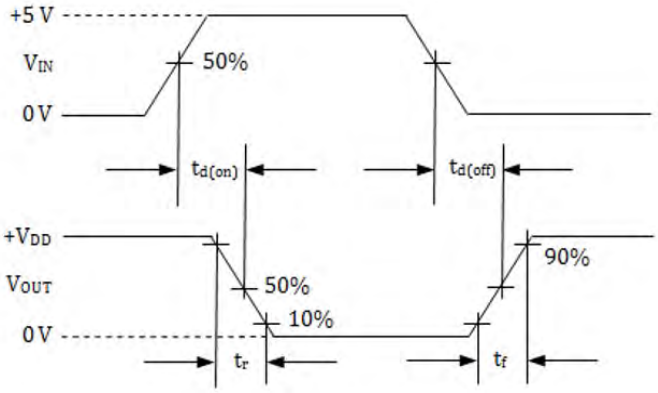
a. T_A = 25°C unless otherwise notes.

b. B is the body (substrate) and $V_{(BR)}$ is breakdown voltage.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Switching Time Test Circuit





LINEAR SYSTEMS

Improved Standard Products®

SD-SST211/213/215

N-CHANNEL LATERAL DMOS SWITCH ZENER PROTECTED

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DS}$ Min (V)	$V_{(GS)th}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD211DE	30	1.5	45 @ V_{GS}=10V	0.5	2
SD213DE	10	1.5	45 @ V_{GS}=10V	0.5	2
SD215DE	20	1.5	45 @ V_{GS}=10V	0.5	2
SST211	30	1.5	50 @ V_{GS}=10V	0.5	2
SST213	10	1.5	50 @ V_{GS}=10V	0.5	2
SST215	20	1.5	50 @ V_{GS}=10V	0.5	2

Features

- Ultra-High Speed Switching—I_{ON}: 1ns
- Ultra-Low Reverse Capacitance: 0.2pF
- Low Guaranteed r_{DS} @5V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

Benefits

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

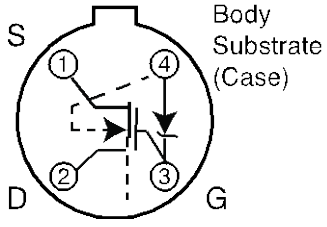
Description

The SD211DE/SST211 series consists of enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video and high-frequency applications. The SD211 may be used for a ±5-V analog switching or as a high speed driver of the SD214. The SD214 is normally used for ±10-V analog switching. These MOSFETs utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. An integrated ZENER diode provides ESD protection. These devices feature a poly-silicon gate for manufacturing reliability.

For similar products see: quad array—SD5000/5400 series, non-Zener protection—SD210DE/214DE.

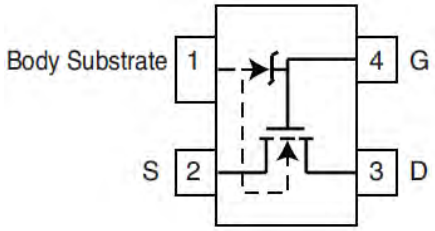
TOP VIEW

SD211DE, SD213DE, SD215DE



TO-206AF
(TO-72)

TO-253
(SOT-143)



TOP VIEW

SST211, SST213, SST215

Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Gate Drain, Gate Source Voltage	(SD211DE/SST211) . . . . . -30/25V	Drain-Substrate Voltage	(SD211DE/SST211) 30V
	(SD213DE/SST213). . . . . -15/25V		(SD213DE/SST213) 15V
	(SD215DE/SST215). . . . . -25/30V		(SD215DE/SST215) 25V
Gate-Substrate Voltage[a]	(SD211DE/SST211) . . . . . -0.3/25V	Source-Substrate Voltage	(SD211DE/SST211) 15V
	(SD213DE/SST213) . . . . . -0.3/25V		(SD213DE/SST213) 15V
	(SD215DE/SST215) . . . . . -0.3/30V		(SD215DE/SST215) 25V
Drain-Source Voltage	(SD211DE/SST211) 30V	Drain Current	. . . . . .50mA
	(SD213DE/SST213) 10V	Lead Temperature (1/16" from ease for 10 seconds)	. . . . . 300°C
	(SD215DE/SST215) 20V	Storage Temperature	. . . . . -65 to 150°C
Voltage	(SD211DE/SST211) 10V	Operating Junction Temperature	. . . . . -55 to 125°C
	(SD213DE/SST213) 10V	Power Dissipation	. . . . . .300mW
	(SD215DE/SST215) 20V		

Notes:
a. Derate 3mW/°C above 25°C

Specifications[a]

PARAMETER	SYMBOL[b]	TEST CONDITIONS[b]		TYP[b]	LIMITS						UNIT
					211 Series		213 Series		215 Series		
					Min	Max	Min	Max	Min	Max	
Static											
Drain - Source Breakdown Voltage	$V_{(BR)DS}$	V_{GS} = V_{BS} = 0V, I_D = 10 µA		35	30						V
		V_{GS} = V_{BS} = -5V, I_D = 10 nA		30	10		10		20		
Source - Drain Breakdown Voltage	$V_{(BR)SD}$	V_{GS} = V_{BD} = -5V, I_S = 10 nA		22	10		10		20		
Drain - Substrate Breakdown Voltage	$V_{(BR)DBO}$	V_{GB} = 0V, I_D= 10 nA Source Open		35	15		15		25		
Source - Substrate Breakdown Voltage	$V_{(BR)SBO}$	V_{GB} = 0V, I_s = 10 µA Drain Open		35	15		15		25		
Drain – Source Leakage	$I_{DS(off)}$	V_{GS} = V_{BS} = -5V	V_{DS} = 10V	0.4		10		10			nA
			V_{DS} = 20V	0.9						10	
Source - Drain Leakage	$I_{SD(off)}$	V_{GD} = V_{BD} = -5V	V_{SD} = 10V	0.5		10		10			
			V_{SD} = 20V							10	
Gate Leakage	I_{GBS}	V_{DB} = V_{SB} = 0V, V_{GB} = 30V		0.01		100		100		100	
Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 µA , V_{SB} = 0V		0.8	0.5	1.5	0.1	1.5	0.1	1.5	V
Drain – Source On-Resistance	$r_{DS(on)}$	V_{SB} = 0V I_D = 1mA	V_{GS} = 5V (SD Series)	58		70		70		70	Ω
			V_{GS} = 5V (SST Series)	60		75		75		75	
			V_{GS} = 10V (SD Series)	38		45		45		45	
			V_{GS} = 10V (SST Series)	40		50		50		50	
			V_{GS} = 15V	30							
			V_{GS} = 20V	26							
			V_{GS} = 25V	24							

Specifications[a]

PARAMETER	SYMBOL[b]	TEST CONDITIONS[b]		TYP[c]	LIMITS						UNIT
					211 Series		213 Series		215 Series		
					Min	Max	Min	Max			
Dynamic											
Forward Transconductance	g_{fs}	V_{DS} = 10V, V_{SB} = 0V, , I_D = 20mA, f = 1kHz	SD Series	11	10		10		10		mS
			SST Series	10.5	9		9		9		
	g_{os}		All	0.9							
Gate Node Capacitance	$C_{(GS+GD+GB)}$	V_{DS} = 10V, f = 1MHz V_{GS} = V_{BS} = -15V	SD Series	2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5		5.5	
Reverse Transfer Capacitance	C_{rss}		SST Series	4.2							
			SD Series	0.2		0.5		0.5		0.5	
Switching											
Turn-On Time	$t_{D(on)}$	SD Series Only V_{SB} = 0V, V_{IN} 0 to 5V, R_G = 25Ω V_{DD} = 5V, R_L = 680Ω		0.5		1		1		1	ns
	t_r			0.6		1		1		1	
Turn-Off Time	$t_{D(off)}$			2							
	t_f			6							

Notes:

a. T_A = 25°C unless otherwise notes.

b. B is the body (substrate) and $V_{(BR)}$ is breakdown voltage.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

LINEAR SYSTEMS

Improved Standard Products®

SD5000/5001/5400/5401

QUAD N-CHANNEL LATERAL DMOS SWITCH ZENER PROTECTED

Product Summary

Part Number	$V_{(BR)DS}$ Min (V)	$V_{GS(th)}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD5000I	20	1.5	70 @ V_{GS} = 5 V	0.5	2
SD5000N	20	1.5	70 @ V_{GS} = 5 V	0.5	2
SD5001N	10	1.5	70 @ V_{GS} = 5 V	0.5	2
SD5400CY	20	1.5	75 @ V_{GS} = 5 V	0.5	2
SD5401CY	10	1.5	75 @ V_{GS} = 5 V	0.5	2

Features

- Quad SPST Switch with Zener Input Protection
- Low Interelectrode Capacitance and Leakage
- Ultra-High Speed Switching—t_{ON}: 1 ns
- Ultra-Low Reverse Capacitance: 0.2 pF
- Low Guaranteed r_{DS} @5 V
- Low Turn-On Threshold Voltage

Benefits

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- Video Switch
- Multiplexer
- DAC Deglitchers
- High-Speed Driver

Description

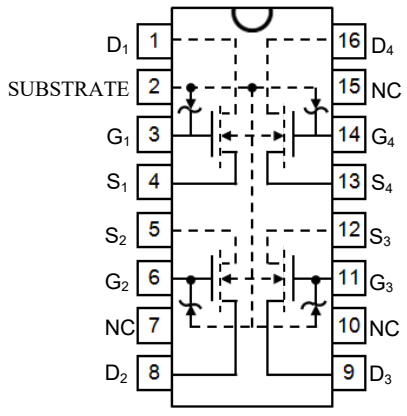
The SD5000/5400 series of monolithic switches features four individual double-diffused enhancement-mode MOSFETs built on a common substrate. These bidirectional devices provide low on-resistance and low interelectrode capacitances to minimize insertion loss and crosstalk.

Built on Siliconix' proprietary DMOS process, the SD5000/5400 series utilizes lateral construction to achieve low capacitance and ultra-fast switching speeds. For manufacturing reliability, these devices feature poly-silicon gates protected by Zener diodes

The SD 5000/5400 are rated to handle ±10-V analog signals, while the SD5001/5401 are rated for ±5-V signals.

For similar products packaged in TO-206AF (TO-72) and TO-253 (SOT-143) see the SD211DE/SST211 series.

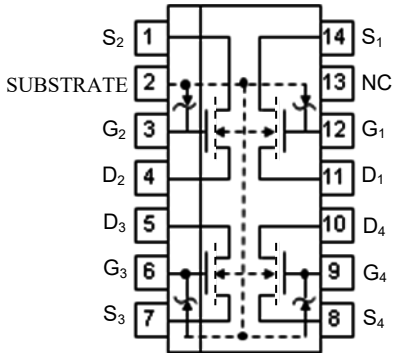
Dual-In-Line



Top View

Plastic: SD5000N
SD5001N
Sidebraze: SD5000I

Narrow Body SOIC



Top View

SD5400CY
SD5401CY

Absolute Maximum Ratings (T_A = 25ºC Unless Otherwise Noted)

Gate-Drain, Gate-Source Voltage
(SD5000, SD5400)……+30V/-25V
(SD5001, SD5401)……+25V/-15V
Gate-Substrate Voltage (SD5000, SD5400)……+30V/-0.3V
(SD5001I, SD5401)……+25V/-0.3V
Drain-Source Voltage (SD5000, SD5400)……20V
(SD5001I, SD5401)……10V
Drain-Source-Substrate Voltage (SD5000, SD5400)……25V
(SD5001I, SD5401)……15V

Drain Current……50 mA
Lead Temperature (1/16" from case for 10 seconds)……300ºC
Storage Temperature……-65 to 150ºC
Operating Junction Temperature……-55 to 150ºC
Power Dissipation": (Package)……500 mW
(each Device)……300 mW

Notes:
a. SD5000/SD5001I derate 5 mW/C above 25ºC
b. SD5400/SD5401 derate 4 mW/C above 25ºC

Specifications[a]

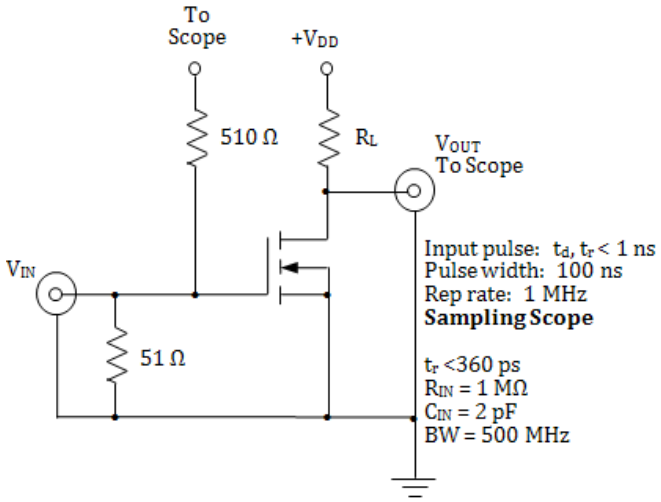
Parameter	Symbol[b]	Test Conditions[b]		Typ[c]	Limits SD5000 SD5400 Min	Limits SD5000 SD5400 Max	Limits SD5001 SD5401 Min	Limits SD5001 SD5401 Max	Unit
Static									
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	V_{GS}=V_{BS}=-5V, I_D=10nA		30	20		10		V
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	V_{GD}=V_{BD}=-5V, I_S=10nA		22	20		10		V
Drain-Substrate Breakdown Voltage	$V_{(BR)DBO}$	V_{GB}=0 V, I_D=10µA, Source Open		35	25		15		V
Source-Substrate Breakdown Voltage	$V_{(BR)SBO}$	V_{GB}=0 V, I_S=10µA, Drain Open		35	25		15		V
Drain-Source Leakage	$I_{DS(off)}$	V_{GS}= V_{BS}=-5 V	V_{DS}= 10 V	0.4				10	nA
			V_{DS}= 15 V	0.7					nA
			V_{DS}= 20 V	0.9		10			nA
Source-Drain Leakage	$I_{SD(off)}$	V_{GD}= V_{BD}=-5 V	V_{SD}= 10 V	0.5				10	nA
			V_{SD}= 15 V	0.8					nA
			V_{SD}= 20 V	1		10			nA
Gate Leakage	I_{GBS}	V_{DB} = V_{SB} = 0 V, V_{GB} =30V		0.01		100		100	nA
Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = I µA, V_{SB} =0V		0.8	0.1	1.5	0.1	1.5	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_{SB} = 0 V, I_D = 1 mA	SD5000 Series V_{GS} = 5 V	58		70		70	Ω
			SD5400 Series V_{GS} = 5 V	60		75		75	Ω
			V_{GS} = 10 V	38					Ω
			V_{GS} = 15 V	30					Ω
			V_{GS} = 20 V	26					Ω
Resistance Match	$\Delta r_{DS(on)}$		V_{GS} = 5 V	1		5		5	Ω
Dynamic									
Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{SB} = 0 V, I_D = 20 mA, f = 1 kHz	SD5000 Series	12	10		10		mS
			SD5400 Series	11	9		9		mS
Gate Node Capacitance	$C_{(GS+GD+GB)}$	V_{DS} = 10 V, f = 1 MHz, V_{GS} = V_{BS} = -15V	SD5000 Series	2.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			2.0		3		3	pF
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5		5	pF
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5	pF
Crosstalk		f = 3 kHz		-107					dB

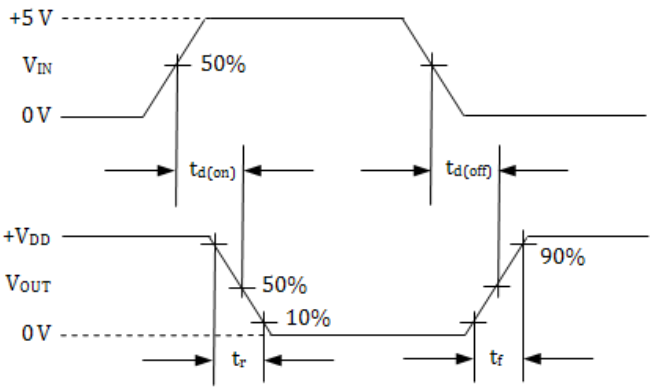
Specifications[a]

Parameter	Symbol[b]	Test Conditions[b]	Typ[c]	Limits				Unit
				SD5000 SD5400		SD5001 SD5401		
				Min	Max	Min	Max	
Switching								
Turn-On Time	$t_{d(on)}$	V_{SB}= 1-5 Vin, V_{GN} 0 to 5 V, R_G = 25 Ω V_{DD} = 5 V, R_L = 680 Ω	0.5		1		1	ns
	t_r		0.6		1		1	
Turn-Off Time	$t_{d(off)}$		2					
	t_f		6					

Notes: DMCA
a. T_A = 25ºC unless otherwise noted.
b. B is the body (substrate) and $V_{(BR)}$ is breakdown.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Switching Time Test Circuit





NOTES:

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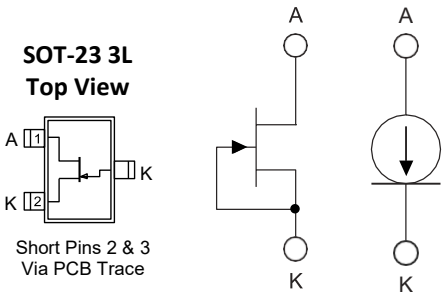
SST500 Series

Current Regulating Diodes

IDEAL CHOICE FOR TEST INSTRUMENTATION AND MEDICAL APPLICATIONS

FEATURES	
REPLACES SILICONIX/VISHAY SST502 SERIES	
WIDE CURRENT RANGE	0.19 to 5.6mA
BIASING NOT REQUIRED	V_{GS} = 0V
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to 150°C
Junction Operating Temperature	-55 to 150°C
Maximum Power Dissipation	
Continuous Power Dissipation[7]	350mW
Maximum Currents	
Forward Current	20mA
Reverse Current	50mA
Maximum Voltages	
Peak Operating Voltage	P_{OV} = 50V



Package Photo

COMMON ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
P_{OV}	Peak Operating Voltage[6]	50			V	$I_F = 1.1I_{F\,(max)}$
V_R	Reverse Voltage		0.8		V	I_R = 1mA
C_F	Forward Capacitance		1.5		pF	V_F = 25V, *f* = 1MHz

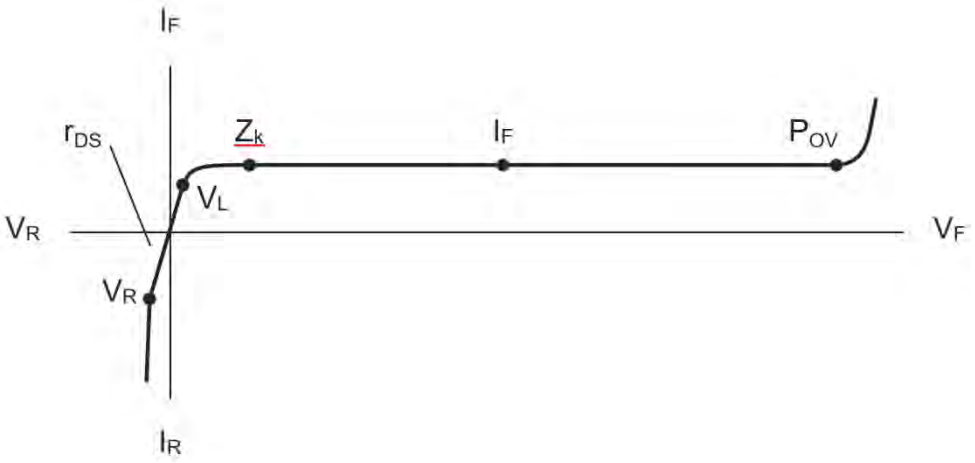
SPECIFIC ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

PART	Forward Current[3] I_F(mA)			Dynamic Impedance[4] Z_d(MΩ)		Knee Impedance Z_k(MΩ)	Limiting Voltage[5] V_L(V)	
	V_F = 25V			V_F = 25V		V_F = 6V	$I_F = 0.8I_{F(min)}$	
	MIN	NOM	MAX	MIN	TYP	TYP	TYP	MAX
SST500	0.192	0.24	0.288	4.00	15	2.50	0.4	1.2
SST501	0.264	0.33	0.396	2.20	10	1.60	0.5	1.3
SST502	0.344	0.43	0.516	1.0	2.7	0.7	0.6	1.5
SST503	0.448	0.56	0.672	0.7	2.0	0.5	0.7	1.7
SST504	0.600	0.75	0.900	0.5	1.5	0.4	0.8	1.9
SST505	0.800	1.00	1.200	0.4	1.0	0.3	0.9	2.1
SST506	1.120	1.40	1.680	0.3	0.8	0.2	1.1	2.5
SST507	1.440	1.80	2.160	0.2	0.6	0.12	1.3	2.8
SST508	1.900	2.40	2.900	0.1	0.4	0.08	1.5	3.1
SST509	2.400	3.00	3.600	0.09	0.3	0.06	1.7	3.5
SST510	2.900	3.60	4.300	0.08	0.3	0.04	1.9	3.9
SST511	3.800	4.70	5.600	0.07	0.2	0.03	2.1	4.2

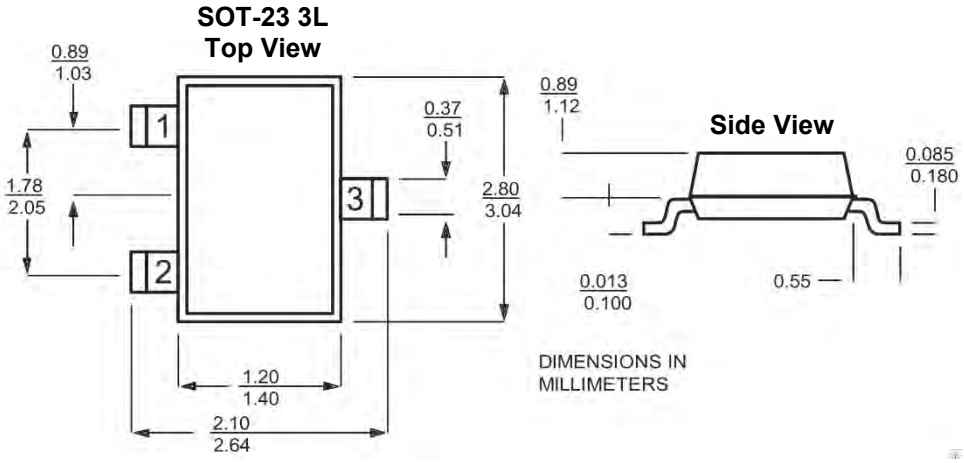
NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulsed, t = 2ms. Steady State currents may vary.
3. Pulsed, t = 2ms. Continuous currents may vary.
4. Pulsed, t = 2ms. Continuous impedances may vary.
5. Min V_F required to ensure $I_F = 0.8I_{F(min)}$.
6. Max V_F where If = 1.1 x I_F max is guaranteed. Pulsed test ≤2mS.
7. Derate 2.8 m W/°C above 25°C.

V-I Characteristics Current Regulating Diode



Packaging Details



Ordering Information

Standard Part Call-Out
SST500 SOT-23 3L RoHS
Custom Part Call-Out (Custom Parts Include SEL + 4 Digit Numeric Code)
SST500 SOT-23 3L RoHS SELXXXX

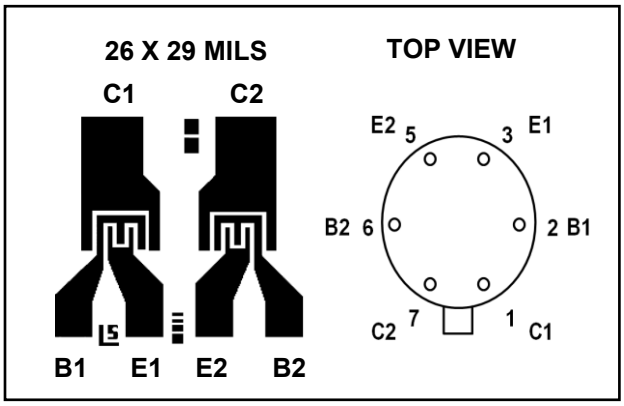
LINEAR SYSTEMS

Improved Standard Products®

IT120A IT120 IT121 IT122

MONOLITHIC DUAL NPN TRANSISTORS

FEATURES		
Direct Replacement for Intersil IT120 Series Pin for Pin Compatible		
ABSOLUTE MAXIMUM RATINGS NOTE 1 (T_A= 25°C unless otherwise noted)		
I_C Collector-Current	10mA	
Maximum Temperatures		
Storage Temperature Range	-65°C to +150°C	
Operating Temperature Range	-55°C to +150°C	
Maximum Power Dissipation	**ONE SIDE**	**BOTH SIDES**
Device Dissipation T_A=25°C	250mW	500mW
Linear Derating Factor	2.3mW/°C	4.3W/°C



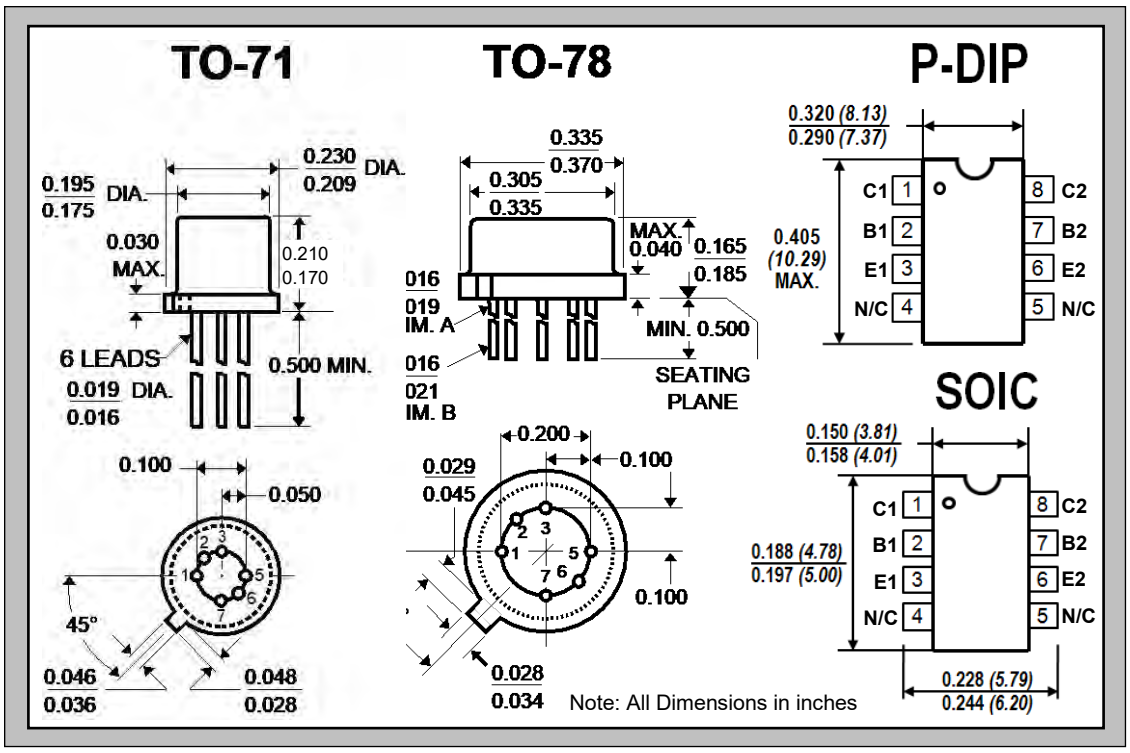
ELECTRICAL CHARACTERISTICS T_A= 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	IT120A	IT120	IT121	IT122		UNITS	CONDITIONS	
BV_{CBO}	Collector to Base Voltage	45	45	45	45	MIN.	V	I_C = 10µA	I_E = 0A
BV_{CEO}	Collector to Emitter Voltage	45	45	45	45	MIN.	V	I_C = 10µA	I_B = 0A
BV_{EBO}	Emitter-Base Breakdown Voltage	6.2	6.2	6.2	6.2	MIN.	V	I_E = 10µA	I_C = 0A **NOTE 2**
BV_{CCO}	Collector to Collector Voltage	60	60	60	60	MIN.	V	I_{CCO} = 10µA	$I_B = I_E$ = 0A
h_{FE}	DC Current Gain	200	200	80	80	MIN.		I_C = 10µA	V_{CE} = 5V
		225	225	100	100	MIN.		I_C = 1.0mA	V_{CE} = 5V
V_{CE}(SAT)	Collector Saturation Voltage	0.5	0.5	0.5	0.5	MAX.	V	I_C = 0.5mA	I_B = 0.05mA
I_{EBO}	Emitter Cutoff Current	1	1	1	1	MAX.	nA	I_C = 0	V_{EB} = 3V
I_{CBO}	Collector Cutoff Current	1	1	1	1	MAX.	nA	I_E = 0	V_{CB} = 45V
C_{OBO}	Output Capacitance[3]	2	2	2	2	MAX.	pF	I_E = 0	V_{CB} = 5V
C_{C1C2}	Collector to Collector Capacitance[3]	2	2	2	2	MAX.	pF	V_{CC} = 0	
I_{C1C2}	Collector to Collector Leakage Current	±500	±500	±500	±500	MAX.	nA	V_{CCO} = ±60V	$I_B = I_E$ = 0A
f_T	Current Gain Bandwidth Product[3]	220	220	180	180	MIN.	MHz	I_C = 1mA	V_{CE} = 5V
NF	Narrow Band Noise Figure[3]	3	3	3	3	MAX.	dB	I_C = 100µA BW = 200Hz, R_G = 10 KΩ f=1KHz	V_{CE} = 5V

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	IT120A	IT120	IT121	IT122		UNITS	CONDITIONS
$\lvert V_{BE1}-V_{BE2}\rvert$	Base Emitter Voltage Differential	1	2	3	5	MAX.	mV	I_C = 10 µA V_{CE} = 5V
$\Delta\lvert (V_{BE1}-V_{BE2})\rvert/\Delta T$	Base Emitter Voltage Differential Change with Temperature[3]	3	5	10	20	MAX.	µV/°C	I_C = 10 µA V_{CE} = 5V T = -55°C to +125°C
$\lvert I_{B1}-I_{B2}\rvert$	Base Current Differential	2.5	5	25	25	MAX.	nA	I_C = 10 µA V_{CE} = 5V

STANDARD PAKAGE DIMENSINS:



NOTES:

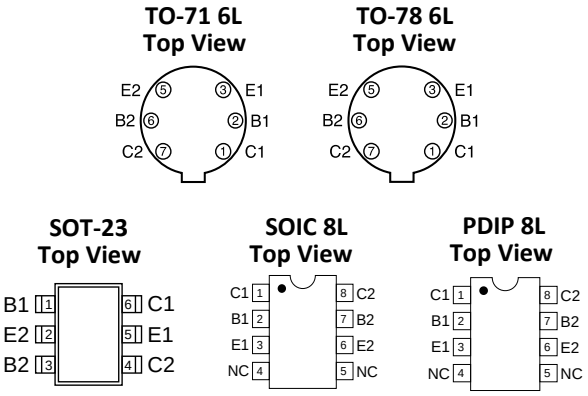
1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. The reverse base-to-emitter voltage must never exceed 6.2 volts; the reverse base-to-emitter current must never exceed 10 µA.
3. Not a production test.

LS3250A/B/C

Monolithic Dual Matched NPN Transistor

LOW NOISE AND THERMALLY MATCHED MONOLITHIC DUAL NPN TRANSISTOR

Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation	400mW
Maximum Voltages	
Maximum Power Supply	45V
Collector to Collector	50V
Maximum Current	
Collector Current	50mA



Features

- Low Voltage Noise, 2.7nV-typ at f=100Hz
- Low Vbe Matching 2mV-max
- Low Vbe Temperature Drift 3µV/˚C-max
- High Current Gain 150-Min and 650-max
- High VCBO Breakdown Voltage-45V-min
- High VCEO Breakdown Voltage-45V-min
- High VCCO Breakdown Voltage +/-50V-min
- Refer to LS350/1/2 dual PNP for counterpart version

Benefits

- Unique Monolithic Dual Design Construction
- Improved System Noise Performance
- Wide Range of Parameter Operations
- High Frequency Performance
- Excellent Matching and Thermal Tracking
- Operation in High Voltage Applications

Applications

- Differential and Preamplifiers
- Multivibrator Circuits
- Music Synthesizers
- Current Sources
- Clocking Networks
- Voltage Controlled Oscillators
- Frequency Division
- Photon Generators

Description

The LS3250A/B/C monolithic dual matched NPN transistor offers excellent matching characteristics and high frequency performance up to 600MHz gain bandwidth product. Low 2pF-max Cobo output capacitance further improves frequency characteristics and decreases signal distortion at the output.

Tight current gain matching and high current gain, make the LS3250 an ideal choice for accurate current biasing and mirroring circuits and designs. LS3250 output stages do not need considerable error correction, due to their higher transconductance and have a positive temperature coefficient of current (Ib and Ic).

Low noise performance, low offset voltage and high bandwidth, make the LS3250 ideal for differential input stages and pre-amplifier applications.

Due to its high breakdown specifications, the LS3250 is suitable in high voltage applications requiring up to 45VMax. In addition to the very small outline SOT-23 6L package, the LS3250 is available in the TO-78 6L, TO-71 6L, PDIP 8L and SOIC 8L packages.

Furthermore, the LS3250 is offered with custom electrical specifications called SELXXXX. Contact our factory for modified electrical specifications for these special versions of the LS3250 SELXXXX.

Refer to the LS350/1/2 dual PNP for the counterpart version.

Electrical Characteristics @ 25 °C (Unless Otherwise Stated)

SYMBOL	CHARACTERISTIC	LS3250A		LS3250B		LS3250C		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
$\lvert V_{BE1} - V_{BE2} \rvert$	Base to Emitter Voltage Differential	-	2	-	5	-	10	mV	I_C = 10µA, V_{CE} = 5V
$\frac{\lvert V_{BE1} - V_{BE2} \rvert}{\Delta T}$	Base to Emitter Voltage Differential Change with Temperature	-	3	-	5	-	15	µV/°C	I_C = 10µA, V_{CE} = 5V T_A = -40°C to +85°C
$\lvert I_{B1} - I_{B2} \rvert$	Base Current Differential	-	10	-	10	-	10	nA	I_C = 10µA, V_{CE} = 5V
$\frac{\lvert I_{B1} - I_{B2} \rvert}{\Delta T}$	Base Current Differential Change with Temperature	-	0.5	-	0.5	-	1.0	nA/°C	I_C = 10µA, V_{CE} = 5V T_A = -40°C to +85°C
h_{FE1}/h_{FE2}	Current Gain Differential	-	10	-	10	-	15	%	I_C = 1mA, V_{CE} = 5V
BV_{CBO}	Collector to Base Breakdown Voltage	45	-	40	-	20	-	V	I_C = 10µA, I_E = 0A
BV_{CEO}	Collector to Emitter Breakdown Voltage	45	-	40	-	20	-		I_C = 10mA, I_B = 0
BV_{CCO}	Collector to Collector Breakdown Voltage	±50	-	±50	-	±50	-		I_C = ±1µA, I_E = I_B= 0A
BV_{EBO}	Emitter to Base Breakdown Voltage[3]	6.0	-	6.0	-	6.0	-		I_E = 10µA, I_C = 0A
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	-	0.35	-	0.35	-	1.2		I_C = 10mA, I_B = 1mA
h_{FE}	DC Current Gain	150	-	100	-	50	-	-	I_C = 1mA, V_{CE} = 5V
		150	650	80	-	40	-		I_C = 10mA, V_{CE} = 5V
		125	-	60	-	30	-		I_C = 35mA, V_{CE} = 5V
I_{CBO}	Collector Cutoff Current	-	0.35	-	0.35	-	-	nA	I_E = 0A, V_{CB} = 30V
		-	-	-	-	-	0.2		I_E = 0A, V_{CB} = 20V
I_{EBO}	Emitter Cutoff Current	-	0.35	-	0.35	-	0.35		I_E = 0A, V_{CB} = 3V
I_{C1C2}	Collector to Collector Leakage Current	-	±1	-	±1	-	±1	µA	V_{CC} = ±50V, I_E = I_B= 0A
C_{OBO}	Output Capacitance	-	2	-	2	-	2	pF	I_E = 0A, V_{CB} = 10V
f_T	Gain Bandwidth Product (Current)	-	600	-	600	-	600	MHz	I_C = 1mA, V_{CE} = 5V
en	Noise Voltage	-	2.7typ	-	2.7typ	-	2.7typ	nV/√Hz	V_{CE}==5V, IC=2mA F=100Hz, NBW=1Hz
en	Noise Voltage	-	0.7typ	-	0.7typ	-	0.7typ	nV/√Hz	V_{CE} ==5V, IC=2mA F=1kHz, NBW=1Hz

Notes

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

Typical Characteristics

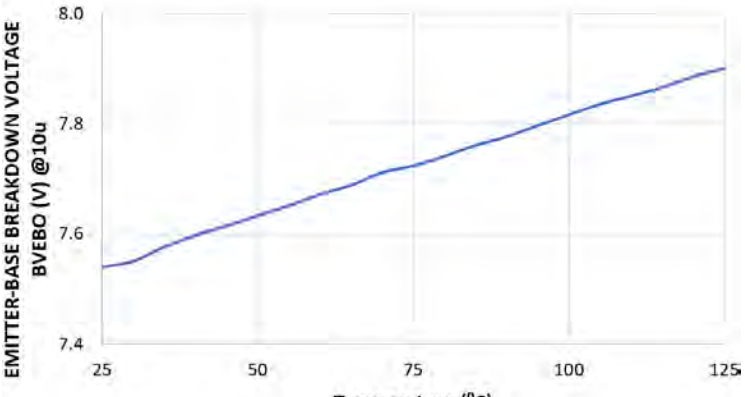


Figure-1 BVEBO(V) vs. Temperature

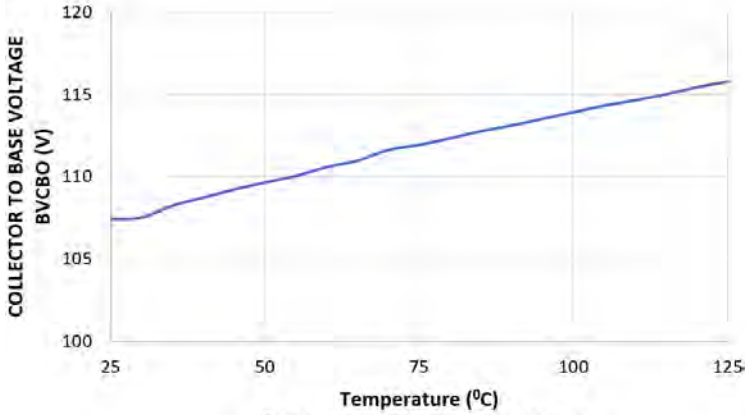


Figure-2 BVCBO(V) vs. Temperature

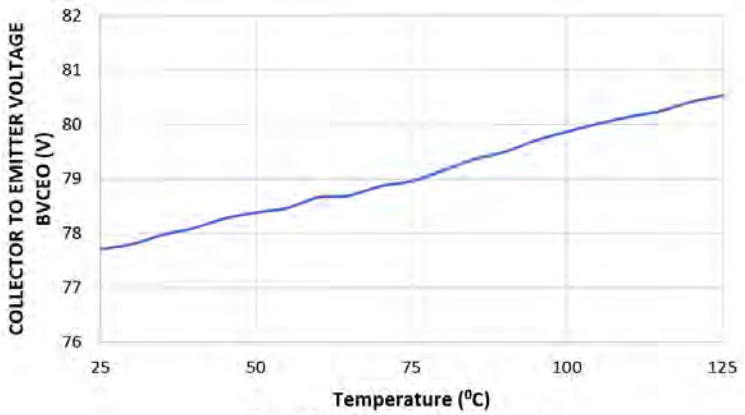


Figure-3 (BVCEO(V) vs. Temperature

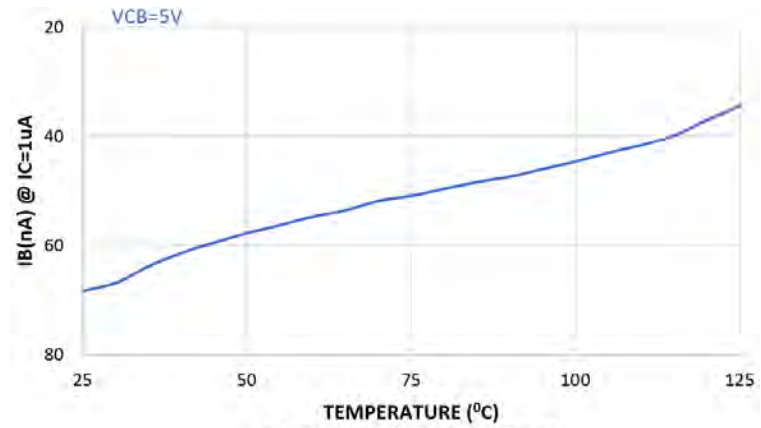


Figure-4 IB(nA) vs. Temperature

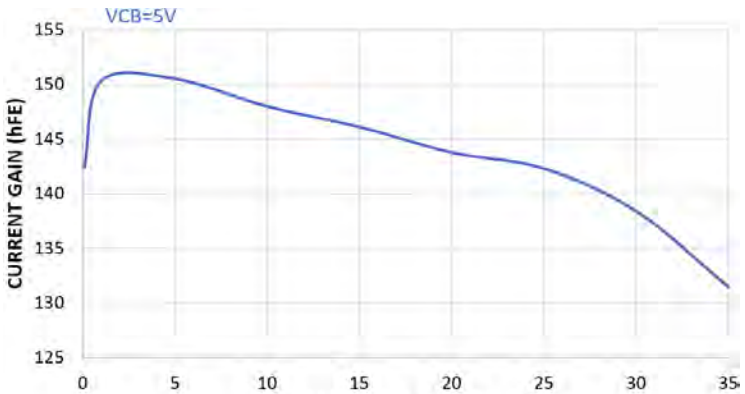


Figure-5 COLLECTOR CURRENT vs. CURRENT GAIN (hFE)

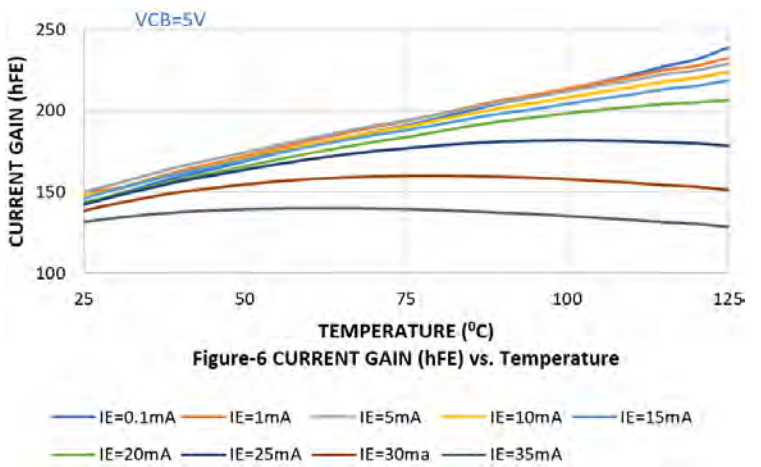


Figure-6 CURRENT GAIN (hFE) vs. Temperature

Typical Characteristics Continued

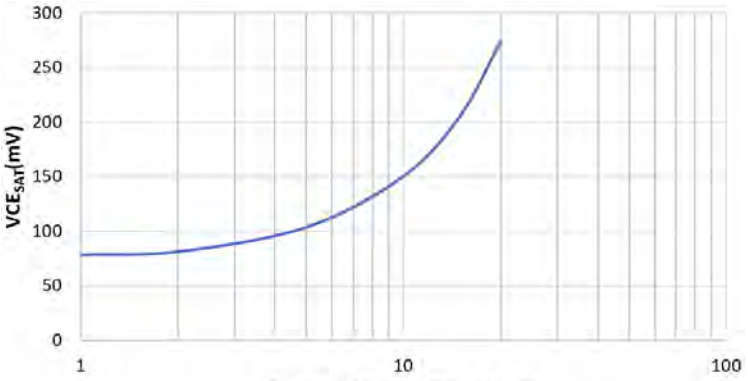


Figure-7 COLLECTOR CURRENT(mA) vs. VCE$_{SAT}$ (mV)

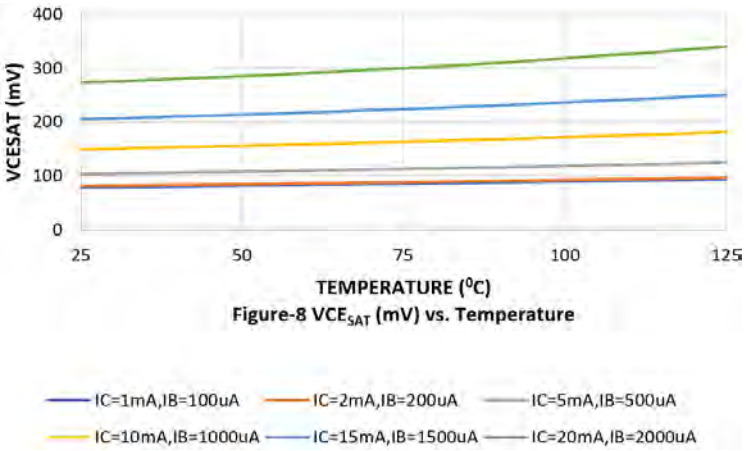


Figure-8 VCE$_{SAT}$ (mV) vs. Temperature

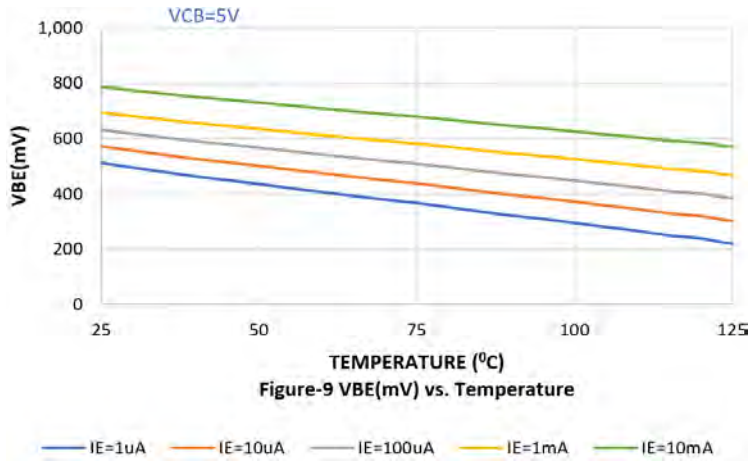


Figure-9 VBE(mV) vs. Temperature

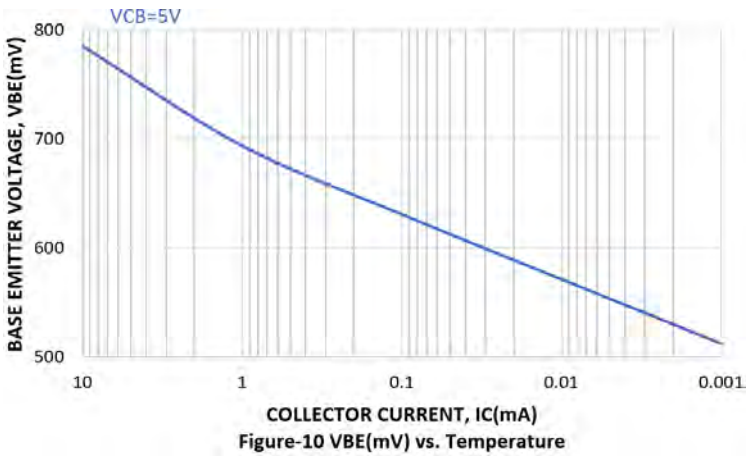


Figure-10 VBE(mV) vs. Temperature

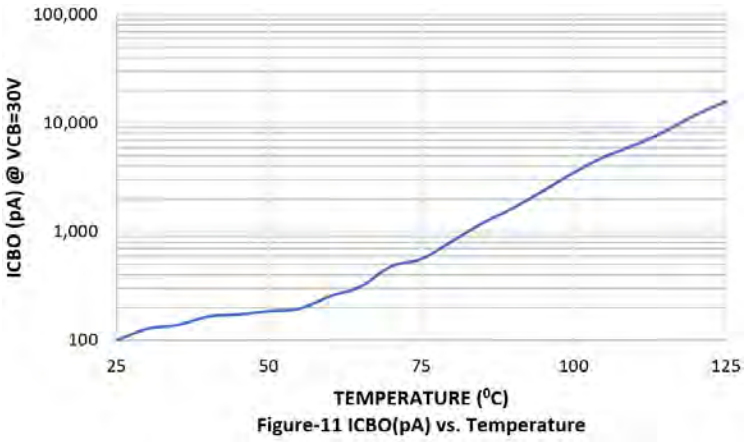


Figure-11 ICBO(pA) vs. Temperature

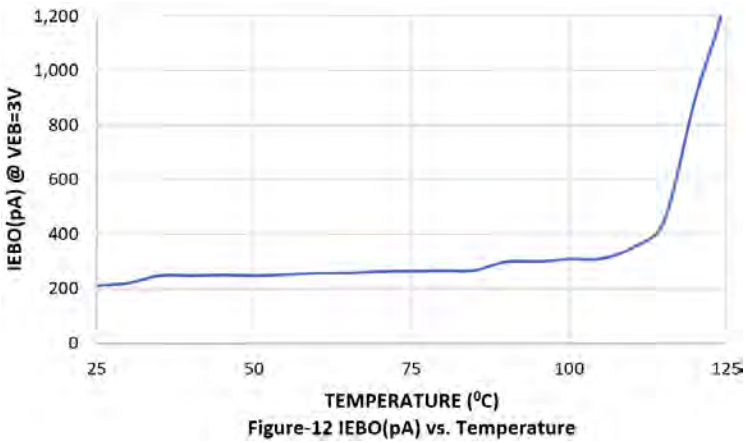


Figure-12 IEBO(pA) vs. Temperature

Typical Characteristics Continued

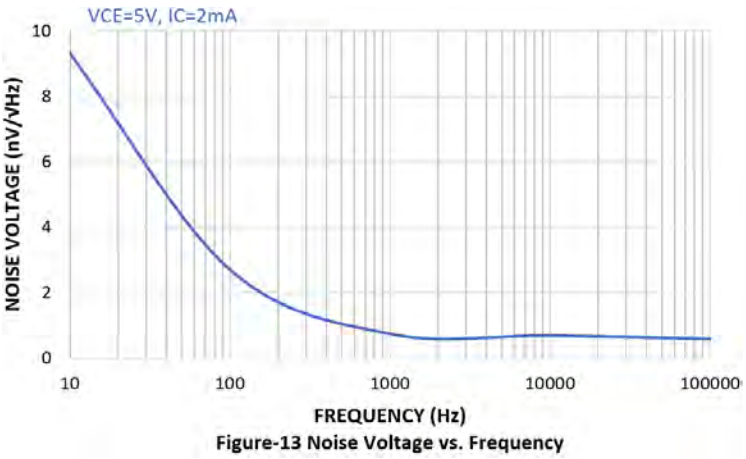


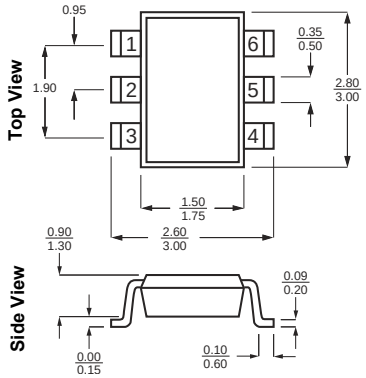
Figure-13 Noise Voltage vs. Frequency

Ordering Information

Standard Part Call-Out
LS3250A/B/C TO-71 6L RoHS
LS3250A/B/C TO-78 6L RoHS
LS3250A/B/C PDIP 8L RoHS
LS3250A/B/C SOIC 8L RoHS
LS3250A/B/C SOT-23 6L RoHS
Custom Part Call-out Custom parts include SEL+4 digit numeric code
LS3250A/B/C TO-71 6L RoHS SELXXXX
LS3250A/B/C TO-78 6L RoHS SELXXXX
LS3250A/B/C PDIP 8L RoHS SELXXXX
LS3250A/B/C SOIC 8L RoHS SELXXXX
LS3250A/B/C SOT-23 6L RoHS SELXXXX

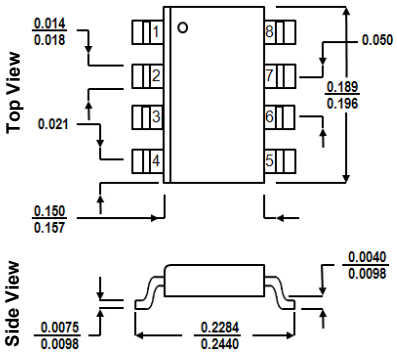
Package Dimensions

SOT-23 6 Lead



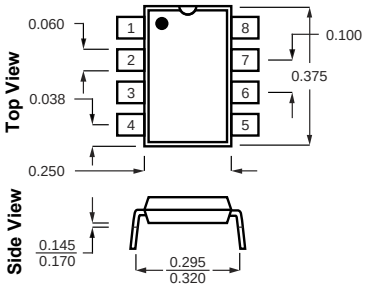
DIMENSIONS IN MILLIMETERS

SOIC-A 8 Lead



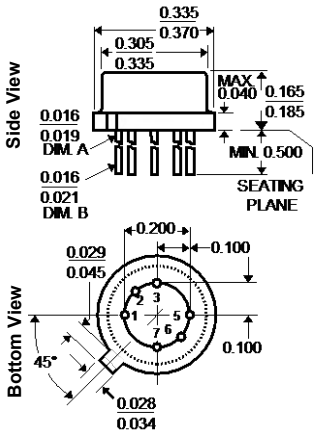
DIMENSIONS IN INCHES

PDIP 8 Lead



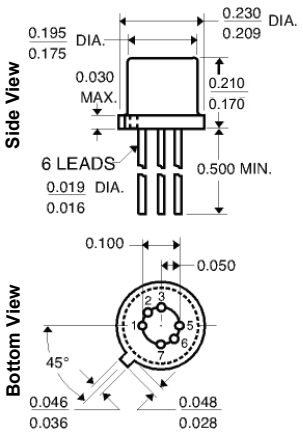
DIMENSIONS IN INCHES

TO-78 6 Lead



DIMENSIONS IN INCHES

TO-71 6 Lead



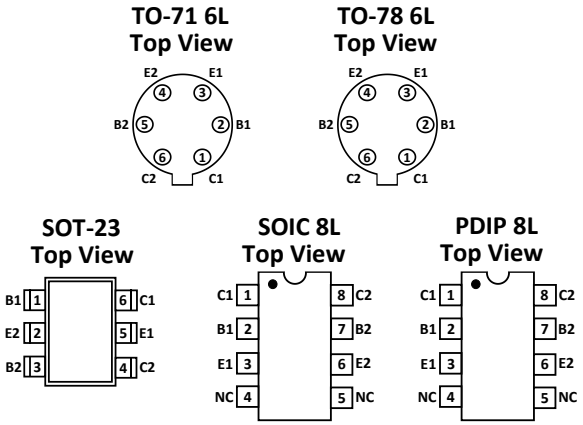
DIMENSIONS IN INCHES

LS310/311/312/313

Monolithic Dual Matched NPN Transistor

LOW NOISE AND THERMALLY MATCHED MONOLITHIC DUAL NPN TRANSISTOR

Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation	400mW
Maximum Voltages	
Maximum Power Supply (LS312, see V_{CEO} for others)	60V
Collector to Collector (LS312, see V_{CEO} for others)	60V
Maximum Current	
Collector Current	40mA



Features

- Low Voltage Noise, 1.8nV/√Hz-typ at f=1kHz, IC=100µA
- Low Vbe Matching 0.5mV-max, 0.2mV-typ (LS312)
- Low Vbe Temperature Drift 0.5 µV/˚C-typ (LS312)
- High Current Gain 400-Min (LS313)
- High VCBO Breakdown Voltage-60V-min (LS312)
- High VCEO Breakdown Voltage-60V-min (LS312)
- High VCCO Breakdown Voltage +/-60V-min
- Dual PNP Counterpart Version: LS350/1/2

Benefits

- Unique Monolithic Dual Design Construction
- Improved System Noise Performance
- Wide Range of Parameter Operations
- Excellent Base-Emitter Voltage Differential (ΔVBE) and Drift
- Excellent Base Current Differential (IB1-IB2) and Drift
- High Frequency Performance
- Excellent Matching and Thermal Tracking
- High Voltage Operation-60V-min (LS312)

Applications

- Input Differential and Preamplifier Stages
- Multivibrator Circuits
- Music Synthesizers
- Current Sources
- Discreate Operational and Instrumentation Amplifiers
- Clocking Networks
- Voltage Controlled Oscillators
- Frequency Division

Description

The LS310/11/12/13 monolithic dual matched NPN transistors offer excellent matching characteristics and low voltage noise (refer to figure-14 for details.)

Low 2pF-max Cobo output capacitance further improves frequency characteristics and decreases signal distortion at the output. Low noise performance, low offset voltage and high bandwidth, make the products ideal for differential input stages and preamplifier applications.

Tight current gain matching, high current gain and high breakdown make the LS312 and LS313 an ideal choice for signal amplifying, accurate current biasing and mirroring circuits and designs.

LS310/11/12/13 output stages need very little error correction, due to their higher transconductance and have a positive temperature coefficient of current (Ib and Ic).

Due to high breakdown specifications, the products are suitable in high voltage applications requiring up to 60VMax. In addition to very small outline SOT-23 6L package, these products are available in TO-78 6L, TO-71 6L, PDIP 8L and SOIC 8L packages.

The LS310/11/12/13 is offered with custom electrical specifications called SELXXXX. Contact the factory for modified electrical specifications for these special versions of the LS310/11/12/13 SEL-XXXX.

Refer to LS350/1/2 products for dual PNP counterpart versions.

LS310 Series

Electrical Characteristics @ 25 °C (Unless Otherwise Stated)

SYMBOL	CHARACTERISTICS	LS310	LS311	LS312	LS313		UNITS	CONDITIONS
BV_{CBO}	Collector to Base Voltage	25	45	60	45	MIN.	V	I_C = 10µA, I_E = 0
BV_{CEO}	Collector to Emitter Voltage	25	45	60	45	MIN.	V	I_C = 1mA, I_B = 0
BV_{EBO}	Emitter-Base Breakdown Voltage	6.0	6.0	6.0	6.0	MIN.	V	I_E = 10µA, I_C = 0
BV_{CCO}	Collector to Collector Voltage	45	45	60	45	MIN.	V	I_C = 10µA, I_E = I_B = 0A
h_{FE}	DC Current Gain	150	150	200	400 1000	MIN. MAX.	--	I_C = 10µA, V_{CE} = 5V
h_{FE}	DC Current Gain	150	150	200	400	MIN.	--	I_C = 100µA, V_{CE} = 5V
h_{FE}	DC Current Gain	150	150	200	400	MIN.	--	I_C = 1mA, V_{CE} = 5V
V_{CE}(SAT)	Collector Saturation Voltage	0.25	0.25	0.25	0.25	MAX.	V	I_C = 1mA, I_B = 0.1mA
I_{CBO}	Collector Cutoff Current	0.2	0.2	0.2	0.2	MAX.	nA	I_E = 0, V_{CB} = 5V
I_{EBO}	Emitter Cutoff Current	0.2	0.2	0.2	0.2	MAX.	nA	I_C = 0, V_{EB} = 3V
C_{OBO}	Output Capacitance	2	2	2	2	MAX.	pF	I_E = 0, V_{CB} = 5V, f = 1MHz
C_{C1C2}	Collector to Collector Capacitance	2	2	2	2	MAX.	pF	V_{CC} = 0V
I_{C1C2}	Collector to Collector Leakage Current	1.0	1.0	1.0	1.0	MAX.	µA	V_{CC} = 30V
f_T	Current Gain Bandwidth Product	200	200	200	200	MIN.	MHz	I_C = 1mA, V_{CE} = 5V
en	Voltage Noise	1.3	1.3	1.3	1.3	TYP.	nV/√Hz	VCE = 5V, IC = 1mA F = 1kHz, NBW = 1Hz
en	Voltage Noise	1.5	1.5	1.5	1.5	TYP.	nV/√Hz	VCE = 5V, IC = 1mA f = 10Hz, NBW = 1Hz
en	Voltage Noise	1.8	1.8	1.8	1.8	TYP.	nV/√Hz	VCE = 5V, IC = 100µA F = 1kHz, NBW = 1Hz
en	Voltage Noise	3.8	3.8	3.8	3.8	TYP.	nV/√Hz	VCE = 5V, IC = 100µA F = 10Hz, NBW = 1Hz

Notes

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

Typical Characteristics

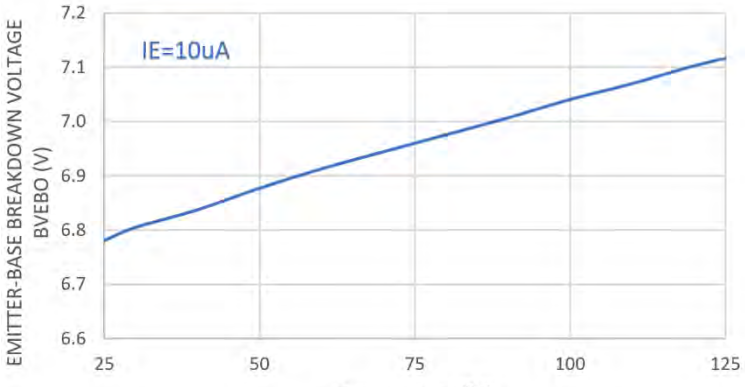


Figure-1 BVEBO(V) vs. Temperature

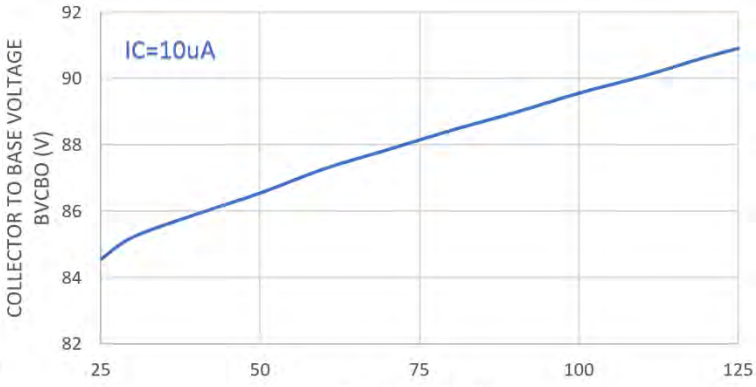


Figure-2 BVCBO(V) vs. Temperature

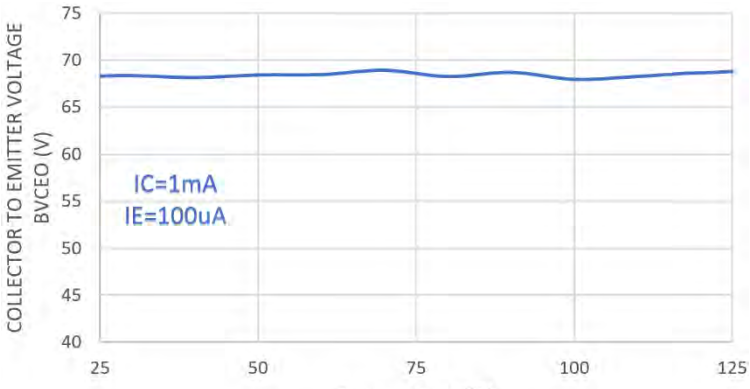


Figure-3 BVCEO(V) vs. Temperature

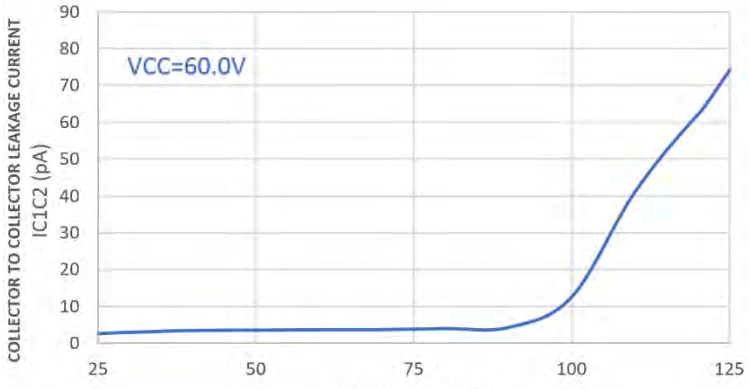


Figure-4 COLLECTOR TO COLLECTOR CURRENT LEAKAGE(pA) vs. Temperature

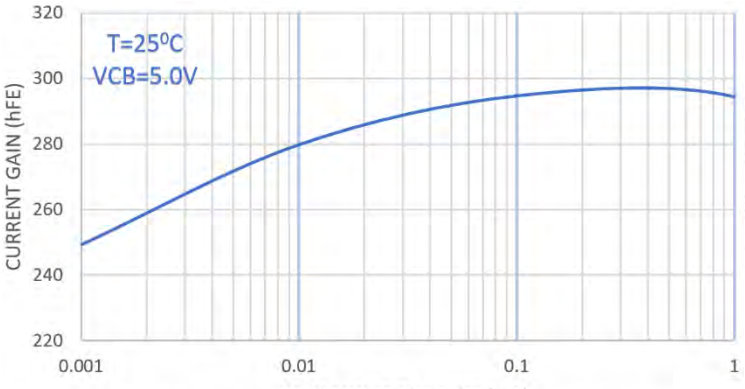


Figure-5 COLLECTOR CURRENT vs. CURRENT GAIN (hFE)

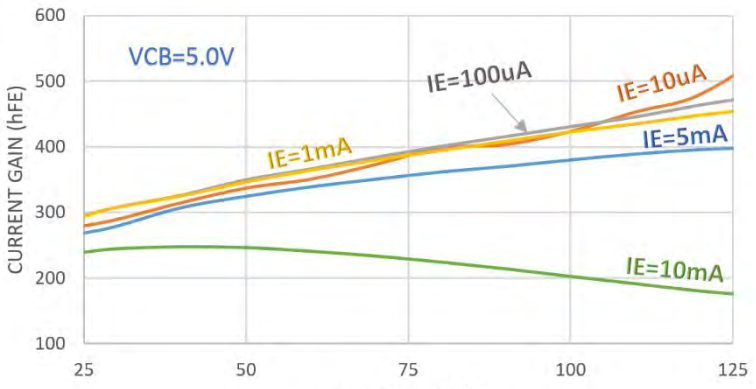


Figure-6 CURRENT GAIN(hFE) vs. Temperature

Typical Characteristics Continued

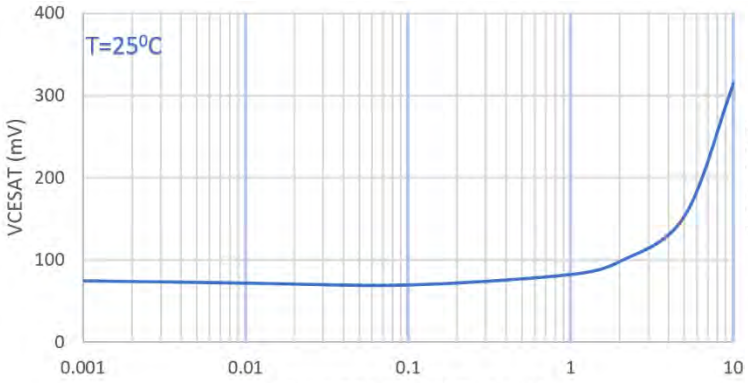


Figure-7 COLLECTOR CURRENT(mA) vs. VCE_{SAT}(mV)

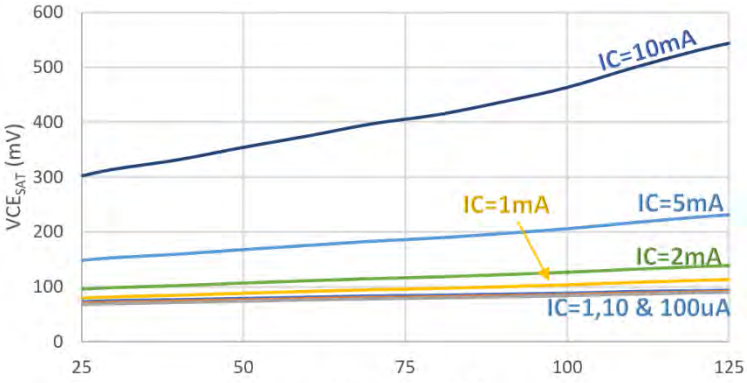


Figure-8 VCE_{SAT}(mV) vs. Temperature

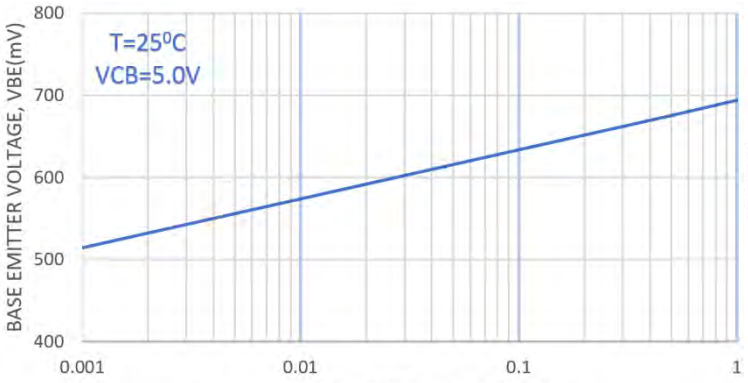


Figure-9 COLLECTOR CURRENT(mA) vs. BASE EMITTER VOLTAGE(V)

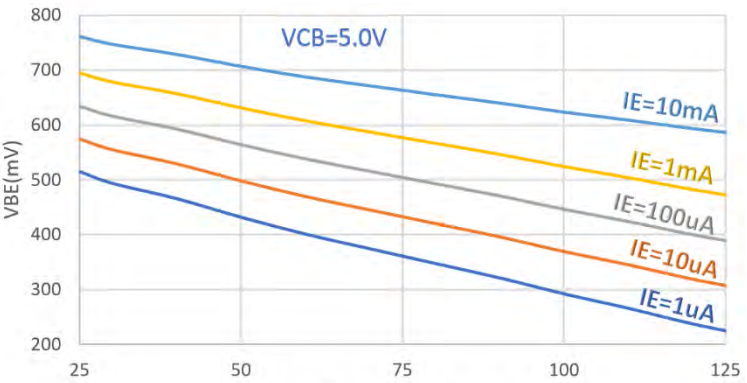


Figure-10 VBE(mV) vs. Temperature

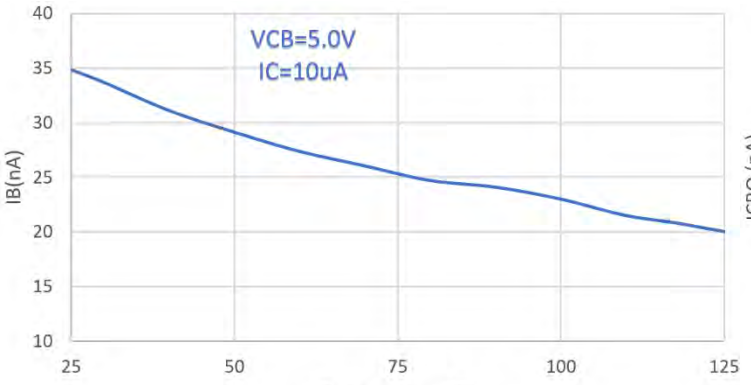


Figure-11 IB(nA) vs. Temperature

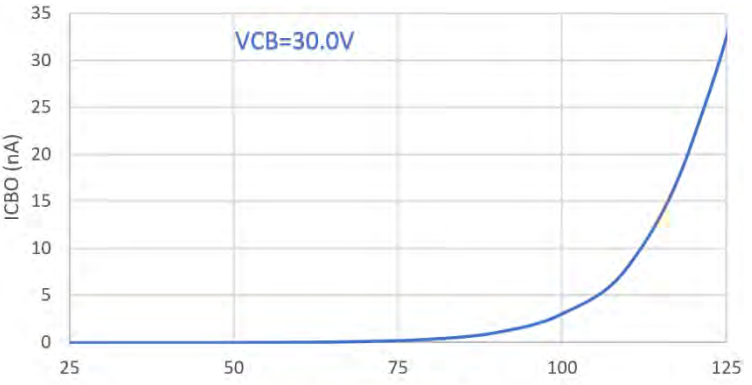


Figure-12 ICBO(nA) vs. Temperature

Typical Characteristics Continued

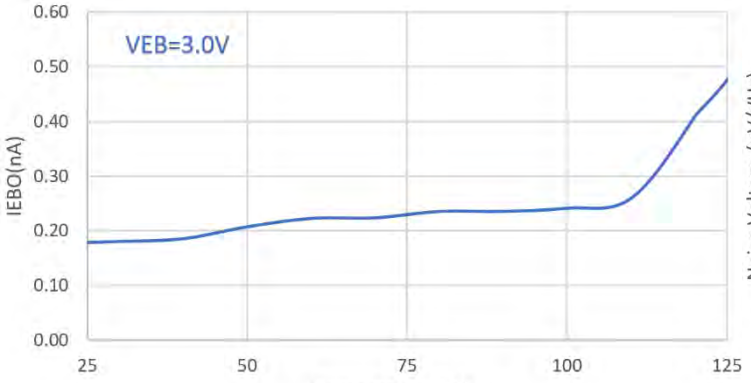


Figure-13 IEBO(nA) vs. Temperature

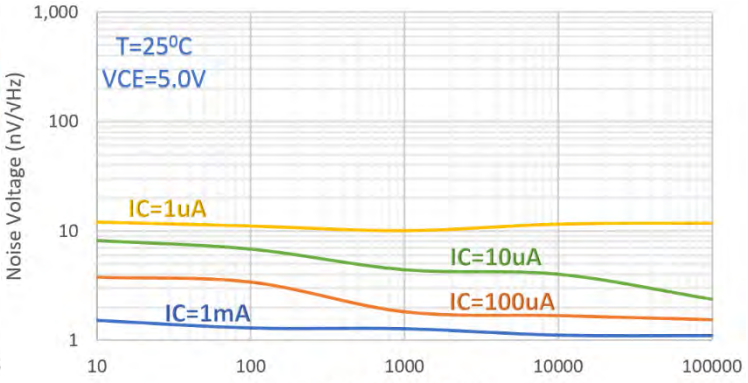


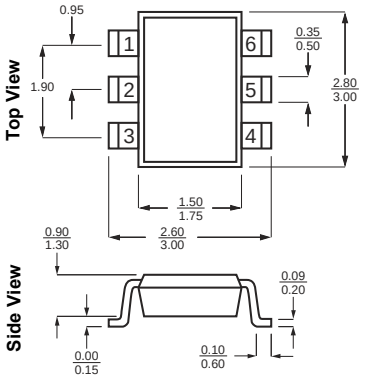
Figure-14 NOISE VOLTAGE vs. FREQUENCY

Ordering Information

Standard Part Call-Out
LS310/311/312/313 TO-71 6L RoHS
LS310/311/312/313 TO-78 6L RoHS
LS310/311/312/313 PDIP 8L RoHS
LS310/311/312/313 SOIC 8L RoHS
LS310/311/312/313 SOT-23 6L RoHS
Custom Part Call-out Custom Parts Include SEL+4 Digit Numeric Code
LS310/311/312/313 TO-71 6L RoHS SELXXXX
LS310/311/312/313 TO-78 6L RoHS SELXXXX
LS310/311/312/313 PDIP 8L RoHS SELXXXX
LS310/311/312/313 SOIC 8L RoHS SELXXXX
LS310/311/312/313 SOT-23 6L RoHS SELXXXX

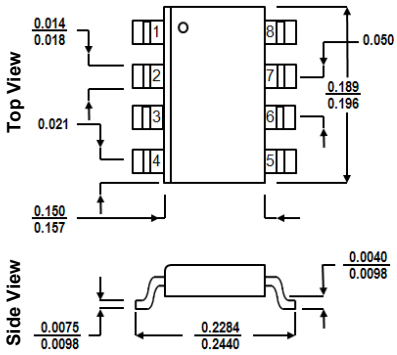
Package Dimensions

SOT-23 6 Lead



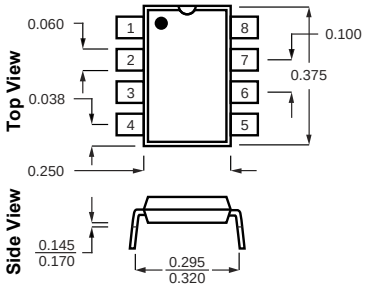
DIMENSIONS IN MILLIMETERS

SOIC-A 8 Lead



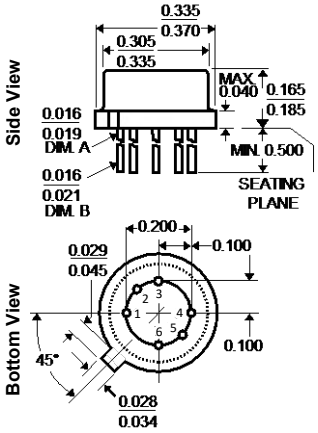
DIMENSIONS IN INCHES

PDIP 8 Lead



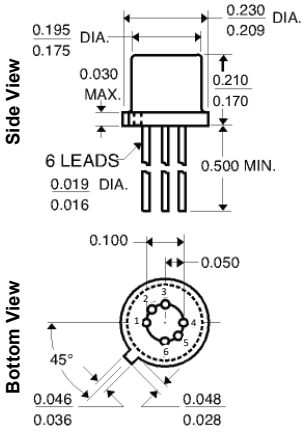
DIMENSIONS IN INCHES

TO-78 6 Lead



DIMENSIONS IN INCHES

TO-71 6 Lead



DIMENSIONS IN INCHES

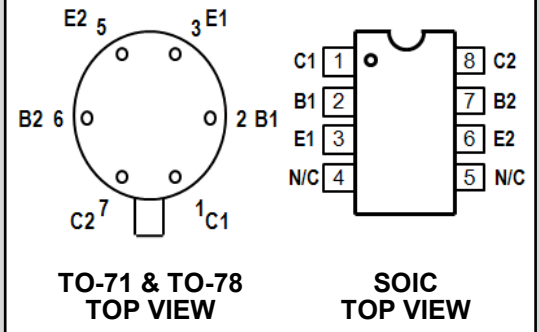
LINEAR SYSTEMS

Improved Standard Products®

LS301 LS302 LS303

HIGH VOLTAGE SUPER-BETA MONOLITHIC DUAL NPN TRANSISTORS

FEATURES		
VERY HIGH GAIN	h_{FE} 2000 @ 1.0μA TYP.	
LOW OUTPUT CAPACITANCE	C_{OBO} 2.0pF	
TIGHT V_{BE} MATCHING	$\lvert V_{BE1}-V_{BE2}\rvert$=0.2mV TYP.	
HIGH f_T	100 MHz	
ABSOLUTE MAXIMUM RATINGS NOTE 1 @ 25 °C (unless otherwise stated)		
I_C	**Collector Current**	**5mA**
Maximum Temperatures		
Storage Temperature	-55 to +150 °C	
Operating Junction Temperature	-55 to +150 °C	
Maximum Power Dissipation	**ONE SIDE**	**BOTH SIDES**
Device Dissipation @ Free Air	250mW	500mW
Linear Derating Factor	2.3mW/°C	4.3mW/°C



TO-71 & TO-78 TOP VIEW **SOIC TOP VIEW**

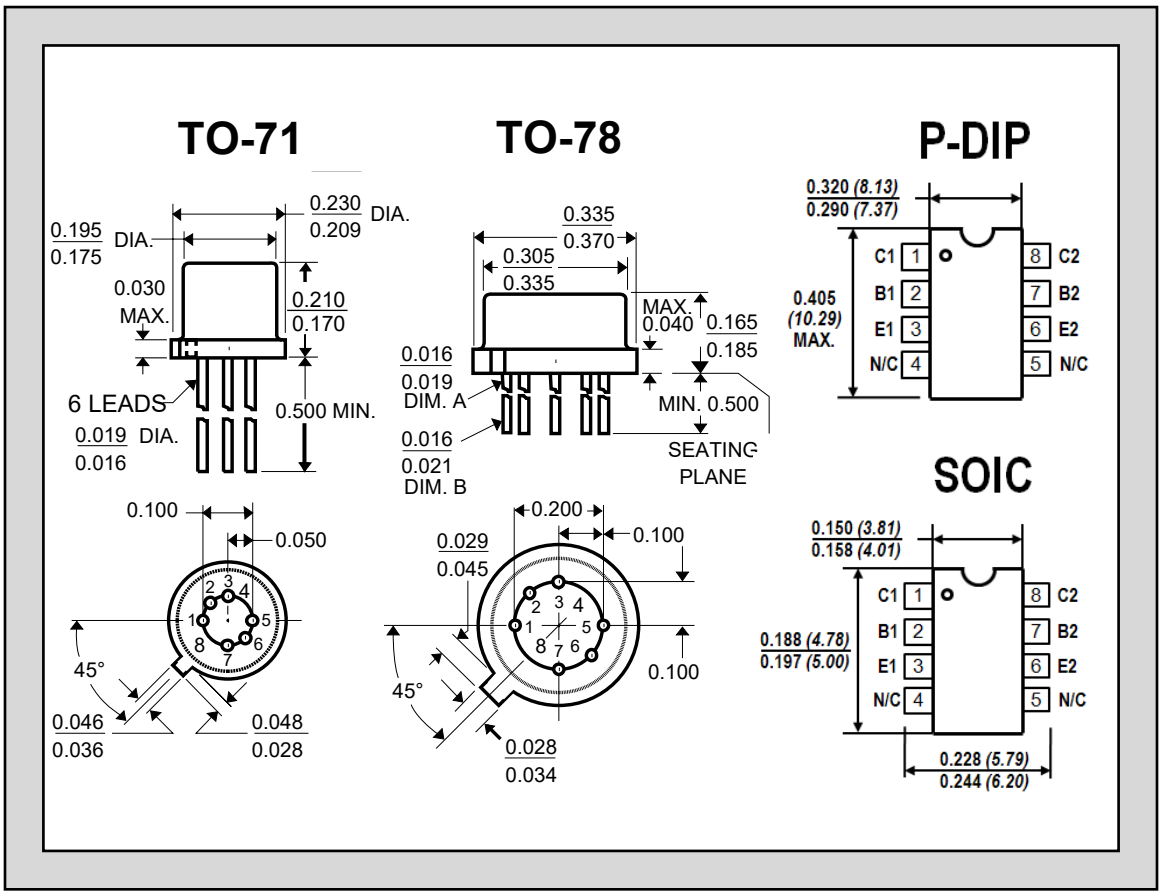
ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	LS301	LS302	LS303		UNITS	CONDITIONS
BV_{CBO}	Collector to Base Voltage	18	35	10	MIN.	V	I_C = 10μA I_E = 0
BV_{CEO}	Collector to Emitter Voltage	18	35	10	MIN.	V	I_C = 1mA I_B = 0
BV_{EBO}	Emitter-Base Breakdown Voltage	6.0	6.0	6.0	MIN.	V	I_E = 10μA I_C = 0 NOTE 2
BV_{CCO}	Collector To Collector Voltage	80	80	20	MIN.	V	I_C = 1μA $I_E = I_B$ = 0
h_{FE}	DC Current Gain	2000	1000	2000	TYP.		I_C = 1μA V_{CE} = 5V
h_{FE}	DC Current Gain	2000	1000	2000	MIN.		I_C = 10μA V_{CE} = 5V
h_{FE}	DC Current Gain	2000	1000	2000	TYP.		I_C = 500μA V_{CE} = 5V
V_{CE}(SAT)	Collector Saturation Voltage	0.5	0.5	0.5	MAX.	V	I_C = 1mA I_B = 0.1mA
I_{CBO}	Collector Cutoff Current	100	100	100	MAX.	pA	I_E = 0 V_{CB} = NOTE 3
I_{EBO}	Emitter Cutoff Current	0.2	0.2	0.2	MAX.	pA	I_E = 0 V_{EB} = 3V
C_{OBO}	Output Capacitance	2	2	2	MAX.	pF	I_E = 0 V_{CB} = 1V
C_{C1C2}	Collector to Collector Capacitance	2	2	2	MAX.	pF	V_{CC} = 0
I_{C1C2}	Collector to Collector Leakage Current	1.0	1.0	1.0	MAX.	μA	V_{CC} = NOTE 4, $I_E = I_B$ = 0
f_T	Current Gain Bandwidth Product	100	100	100	MIN.	MHz	I_C = 200μA V_{CE} = 5V
NF	Narrow Band Noise Figure	3	3	3	MAX.	dB	I_C = 10μA V_{CE} = 3V BW = 200Hz R_G = 10K f = 1KHz

MATCHING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	LS301	LS302	LS303		UNITS	CONDITIONS
$\lvert V_{BE1}-V_{BE2}\rvert$	Base Emitter Voltage Differential	0.2	0.2	0.2	TYP.	mV	I_C = 10µA V_{CE} = 5V
		1	1	1	MAX.	mV	
$\lvert(V_{BE1}-V_{BE2})\rvert/°C$	Base Emitter Voltage Differential	1	1	1	TYP.	µV/°C	I_C = 10µA V_{CE} = 5V
	Change with Temperature	5	5	5	MAX.	µV/°C	T = 55°C to +125°C
$\lvert I_{B1}- I_{B2}\rvert$	Base Current Differential	0.5	1	0.5	TYP.	nA	I_C = 10µA V_{CE} = 1V
		1	5	1.5	MAX.	nA	I_C = 10µA V_{CE} = 5V
h_{FE1}/h_{FE2}	DC Current Gain Differential	5	5	5	TYP.	%	I_C = 10µA V_{CE} = 5V

STANDARD PACKAGE DIMENSIONS:



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired
2. The reverse base-to-emitter voltage must never exceed 6.0 volts; the reverse base-to-emitter current must never exceed 10 µAmps.
3. For LS301 & LS302: V_{CB}=10V; for LS303: V_{CB}=5V
4. For LS301 & LS302: V_{CC}=±80V; for LS303: V_{CC}=±20V

LINEAR SYSTEMS

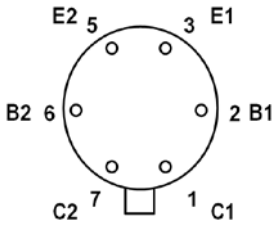
Improved Standard Products®

LS318

LOG CONFORMANCE MONOLITHIC DUAL NPN TRANSISTORS

FEATURES		
LOG CONFORMANCE		Δre =1 TYP.
ABSOLUTE MAXIMUM RATINGS NOTE 1 (T_A= 25°C unless otherwise noted)		
I_C	Collector-Current	10mA
Maximum Temperatures		
Storage Temperature Range		-55°C to +150°C
Operating Junction Temperature		-55°C to +150°C

Maximum Power Dissipation	ONE SIDE	BOTH SIDES
Device Dissipation T_A=25°C	250mW	500mW
Linear Derating Factor	2.3mW/°C	4.3mW/°C



TO 71 & TO 78
TOP VIEW

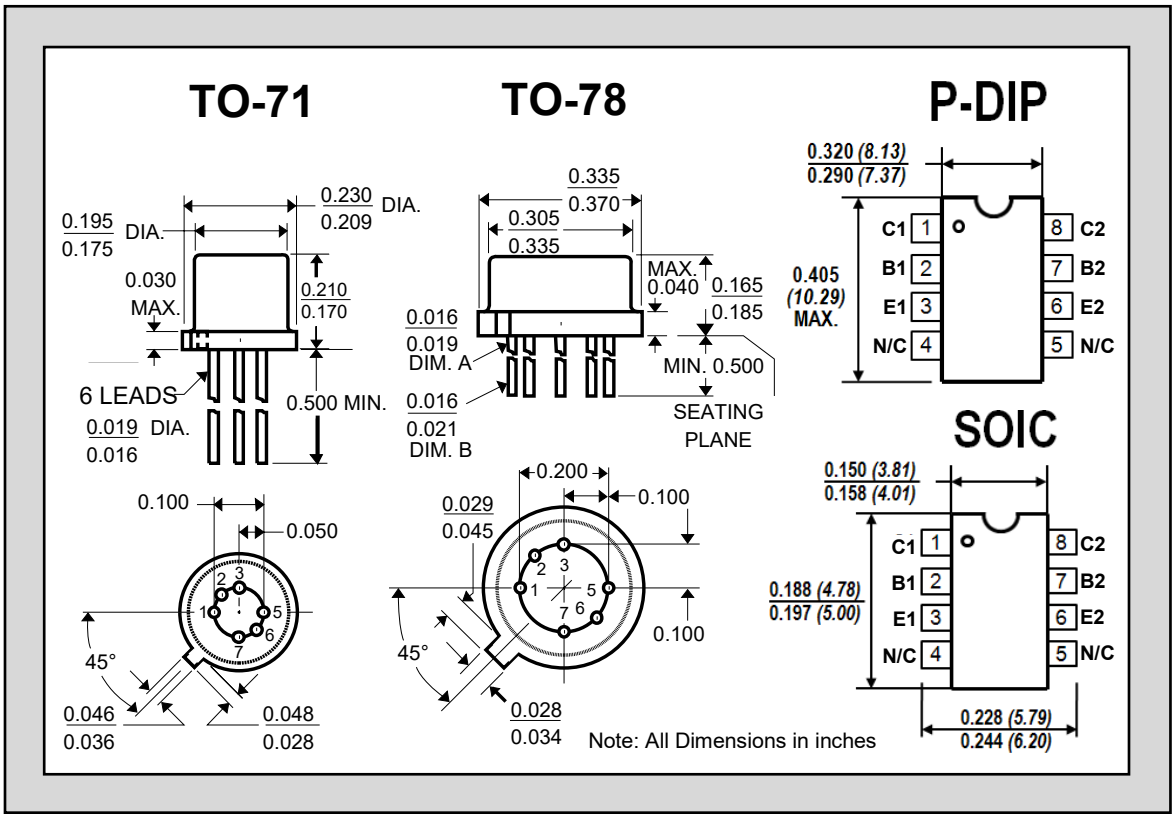
ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS318		UNITS	CONDITIONS
Δre	Log Conformance	1.5	MAX.	Ω	I_C = 10-100-1000μA V_{CE} = 5V
BV_{CBO}	Collector-Base Breakdown Voltage	25	MIN.	V	I_C = 10μA I_E = 0A
BV_{CEO}	Collector to Emitter Voltage	25	MIN.	V	I_C = 100μA I_B = 0A
BV_{EBO}	Emitter-Base Breakdown Voltage	6.0	MIN.	V	I_E = 10μA I_C = 0A **NOTE 2**
BV_{CCO}	Collector to Collector Voltage	45	MIN.	V	I_C = 10μA I_B = I_E =0A
h_{FE}	DC Current Gain	150 600	MIN. MAX.		I_C = 10μA V_{CE} = 5V
h_{FE}	DC Current Gain	150 600	MIN. MAX.		I_C = 100μA V_{CE} = 5V
h_{FE}	DC Current Gain	150	MIN.		I_C = 1mA V_{CE} = 5V
V_{CE}(SAT)	Collector Saturation Voltage	0.25	MAX.	V	I_C = 1mA I_B = 0.1 mA
I_{CBO}	Collector Cutoff Current	0.2	MAX.	nA	I_E = 0A V_{CB} = 20V
I_{EBO}	Emitter Cutoff Current	0.2	MAX.	nA	I_C = 0A V_{EB} = 3V
C_{OBO}	Output Capacitance	1.8		pF	I_E = 0A V_{CB} = 3V f=1MHz **NOTE 3**
C_{C1C2}	Collector to Collector Capacitance	1.8		pF	V_{CC} = 0V f=1MHz **NOTE 3**
I_{C1C2}	Collector to Collector Leakage Current	0.5	MAX.	μA	V_{CC} = ±45V I_B = I_E = 0A
f_T	Current Gain Bandwidth Product	220		MHz	I_C = 1mA V_{CE} = 5V **NOTE 3**
NF	Narrow Band Noise Figure	3	MAX.	dB	I_C = 100μA V_{CE} = 5V **NOTE 3** BW = 200Hz, R_G = 10 K f=1KHz

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS318		UNITS	CONDITIONS
$\lvert V_{BE1}-V_{BE2}\rvert$	Base Emitter Voltage Differential	0.4 1	TYP. MAX.	mV mV	I_C = 10 µA V_{CE} = 5V
$\lvert (V_{BE1}-V_{BE2})\rvert$ /ºC	Base Emitter Voltage Differential Change with Temperature	1	TYP.	µV/°C	I_C = 10 µA V_{CE} = 5V T_A = -55°C to +125°C
$\lvert I_{B1}-I_{B2}\rvert$	Base Current Differential	10	MAX.	nA	I_C = 10 µA V_{CE} = 5V
$\lvert (I_{B1}-I_{B2})\rvert$ /ºC	Base Current Differential Change with Temperature	0.4	TYP.	nA/ºC	I_C = 10 µA V_{CE} = 5V T_A = -55°C to +125°C
h_{FE1}/h_{FE2}	DC Current Gain Differential	5	TYP.	%	I_C = 10 µA V_{CE} = 5V

STANDARD PACKAGE DIMENSIONS:



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. The reverse base-to-emitter voltage must never exceed 6.2 volts; the reverse base-to-emitter current must never exceed 10 µA.
3. Not tested; guaranteed by design.
4. All MIN/TYP/MAX values are absolute numbers. Negative signs indicate electrical polarity only.

LINEAR SYSTEMS

Improved Standard Products®

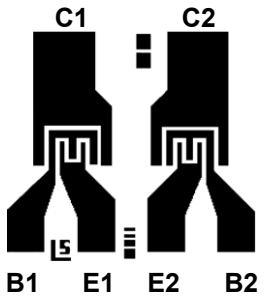
IT130A IT130 IT131 IT132

MONOLITHIC DUAL PNP TRANSISTORS

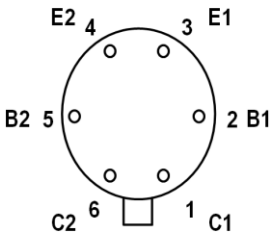
FEATURES
Direct Replacement for Intersil IT130 Series Pin for Pin Compatible

ABSOLUTE MAXIMUM RATINGS NOTE 1 (T_A= 25°C unless otherwise noted)		
I_C	Collector-Current	-10mA
Maximum Temperatures		
Storage Temperature Range		-65°C to +150°C
Operating Junction Temperature		-55°C to +150°C

Maximum Power Dissipation	ONE SIDE	BOTH SIDES
Device Dissipation T_A=25°C	250mW	500mW
Linear Derating Factor	2.3mW/°C	4.3W/°C



26 X 29 MILS



TOP VIEW

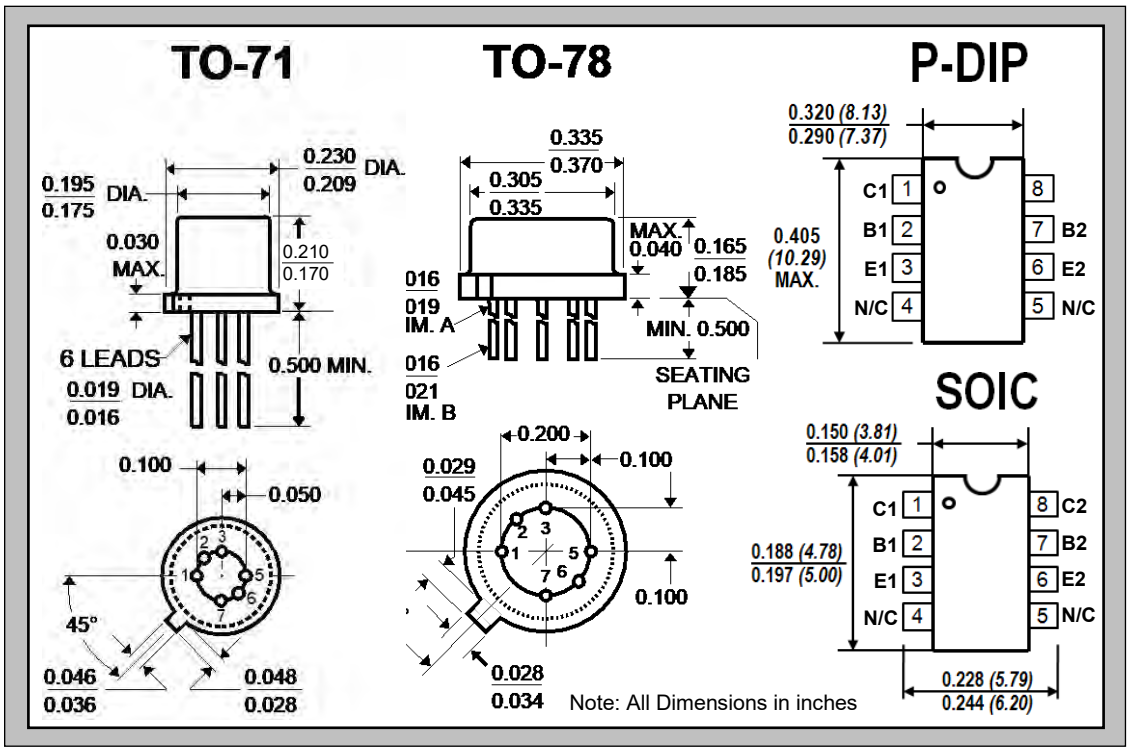
ELECTRICAL CHARACTERISTICS T_A= 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	IT130A	IT130	IT131	IT132		UNITS	CONDITIONS
BV_{CBO}	Collector to Base Voltage	-45	-45	-45	-45	MIN.	V	I_C = -10µA I_E = 0A
BV_{CEO}	Collector to Emitter Voltage	-45	-45	-45	-45	MIN.	V	I_C = -10µA I_B = 0A
BV_{EBO}	Emitter-Base Breakdown Voltage	-6.2	-6.2	-6.2	-6.2	MIN.	V	I_E = -10µA I_C = 0A **NOTE 2**
BV_{CCO}	Collector to Collector Voltage	±60	±60	±60	±60	MIN.	V	I_{CCO} = ±10µA I_B= I_E=0A
h_{FE}	DC Current Gain	200	200	80	80	MIN.		I_C = -10µA V_{CE} = -5V
		225	225	100	100	MIN.		I_C = -1.0mA V_{CE} = -5V
V_{CE}(SAT)	Collector Saturation Voltage	-0.5	-0.5	-0.5	-0.5	MAX.	V	I_C = -0.5mA I_B = -0.05mA
I_{EBO}	Emitter Cutoff Current	-1	-1	-1	-1	MAX.	nA	I_C = 0A V_{EB} = -3V
I_{CBO}	Collector Cutoff Current	-1	-1	-1	-1	MAX.	nA	I_E = 0A V_{CB} = -45V
C_{OBO}	Output Capacitance[4]	2	2	2	2	MAX.	pF	I_E = 0A V_{CB} = -5V
C_{C1C2}	Collector to Collector Capacitance[4]	4	4	4	4	MAX.	pF	V_{CC} = 0V
I_{C1C2}	Collector to Collector Leakage Current	±500	±500	±500	±500	MAX.	nA	V_{CC} = ±60V, I_B= I_E=0A
f_T	Current Gain Bandwidth Product[4]	110	110	90	90	MIN.	MHz	I_C = -1mA V_{CE} = -5V
NF	Narrow Band Noise Figure[4]	3	3	3	3	MAX.	dB	I_C = -100µA V_{CE} = -5V BW = 200Hz, R_G = 10 KΩ f=1KHz

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	IT130A	IT130	IT131	IT132		UNITS	CONDITIONS
$\lvert V_{BE1}-V_{BE2}\rvert$	Base Emitter Voltage Differential	1	2	3	5	MAX.	mV	I_C = -10 µA V_{CE} = -5V
$\Delta\lvert (V_{BE1}-V_{BE2})\rvert/\Delta T$	Base Emitter Voltage Differential	3	5	10	20	MAX.	µV/°C	I_C = 10 µA V_{CE} = 5V
	Change with Temperature[4]							T = -55°C to +125°C
$\lvert I_{B1}-I_{B2}\rvert$	Base Current Differential	2.5	5	25	25	MAX.	nA	I_C = -10 µA V_{CE} = -5V

STANDARD PACKAGE DIMENSIONS:



NOTES:

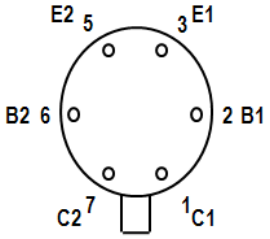
1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. The reverse base-to-emitter voltage must never exceed 6.2 volts; the reverse base-to-emitter current must never exceed 10 µA.
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate electrical polarity only.
4. Not a production test.

LS350, LS351 & LS352

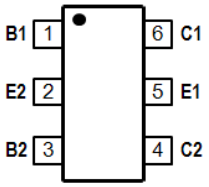
Monolithic Dual PNP Transistors

GENERAL PURPOSE

FEATURES		
HIGH GAIN	h_{FE} 200 @ 10µA - 1mA	
TIGHT V_{BE} MATCHING	$\|V_{BE1}-V_{BE2}\|$=0.2mV TYP.	
HIGH f_T	275 MHz TYP. @ 1mA	
ABSOLUTE MAXIMUM RATINGS NOTE 1 @ 25 °C (unless otherwise stated)		
I_C	**Collector Current**	**10mA**
Maximum Temperatures		
Storage Temperature	-55° to +150°C	
Operating Junction Temperature	+150°C	
Maximum Power Dissipation	**ONE SIDE**	**BOTH SIDES**
Device Dissipation @ Free Air	250mW	500mW
Linear Derating Factor	2.3mW/°C	4.3mW/°C



TO-71 & TO-78 6L
Top View



SOT-23 6 L
Top View

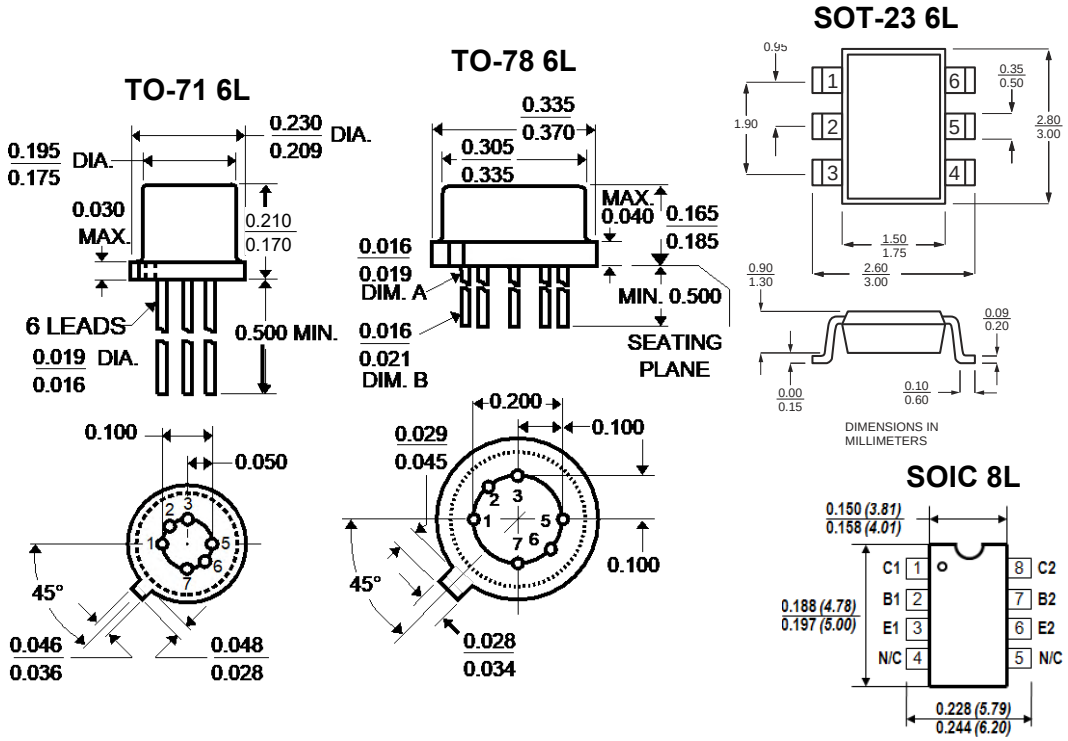
ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	LS350	LS351	LS352		UNITS	CONDITIONS
BV_{CBO}	Collector to Base Voltage	25	45	60	MIN.	V	I_C = 10µA I_E = 0
BV_{CEO}	Collector to Emitter Voltage	25	45	60	MIN.	V	I_C = 1mA I_B = 0
BV_{EBO}	Emitter to Base Voltage	6.0	6.0	6.0	MIN.	V	I_E = 10µA I_C = 0 NOTE 2
BV_{CCO}	Collector to Collector Voltage	±25	±45	±80	MIN.	V	I_C = ±1µA I_E = 0 = I_B = 0
h_{FE}	DC Current Gain	100 600	150 600	200 600	MIN. MAX.		I_C = 10µA V_{CE} = 5V
h_{FE}	DC Current Gain	100 600	150 600	200 600	MIN. MAX.		I_C = 100µA V_{CE} = 5V
h_{FE}	DC Current Gain	100	150	200	MIN.		I_C = 1mA, V_{CE} = 5V
V_{CE}(SAT)	Collector Saturation Voltage	0.5	0.5	0.5	MAX.	V	I_C = 1mA I_B = 0.1mA
I_{CBO}	Collector Cutoff Current	0.2	0.2	0.2	MAX.	nA	I_E = 0 V_{CB} = NOTE 3
I_{EBO}	Emitter Cutoff Current	0.2	0.2	0.2	MAX.	nA	I_C = 0 V_{EB} = 3V
C_{OBO}	Output Capacitance	2	2	2	MAX.	pF	I_E = 0 V_{CB} = 5V
C_{C1C2}	Collector to Collector Capacitance	2	2	2	MAX.	pF	V_{CC} = 0
I_{C1C2}	Collector to Collector Leakage Current	1.0	1.0	1.0	MAX.	µA	V_{CC} = NOTE 4
f_T	Current Gain Bandwidth Product	200	200	200	MIN.	MHz	I_C = 1mA V_{CE} = 5V
NF	Narrow Band Noise Figure	3	3	3	MAX.	dB	I_C = 100µA V_{CE} = 5V BW = 200Hz R_G = 10K f = 1KHz

MATCHING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	LS350 SOT-23	LS351	LS352		UNITS	CONDITIONS
$\lvert V_{BE1}-V_{BE2}\rvert$	Base Emitter Voltage Differential	1	0.4	0.2	TYP.	mV	I_C = 10 µA V_{CE} = 5V
		5	1.0	0.5	MAX.	mV	
$\lvert(V_{BE1}-V_{BE2})\rvert$/°C	Base Emitter Voltage Differential	2	1	0.5	TYP.	µV/°C	I_C = 10 µA V_{CE} = 5V
	Change with Temperature	20	10	2	MAX.	µV/°C	T_A = -55°C to +125°C
$\lvert I_{B1}- I_{B2}\rvert$	Base Current Differential		5	5	MAX.	nA	I_C = 10µA V_{CE} = 5V
$\lvert(I_{B1}- I_{B2})\rvert$/°C	Base Current Differential		0.5	0.3	MAX.	nA/°C	I_C = 10 µA, V_{CE} = 5V
	Change with Temperature						T_A = -55°C to +125°C
h_{FE1}/h_{FE2}	DC Current Gain Differential	10	5	5	TYP.	%	I_C = 10µA V_{CE} = 5V

STANDARD PACKAGE DIMENSIONS



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired
2. The reverse base-to-emitter voltage must never exceed 6.0 volts; the reverse base-to-emitter current must never exceed 10 µA.
3. For LS350: V_{CB}=20V; for LS351 & LS352: V_{CB}=30V.
4. For LS351: V_{CC}=±45V; for LS352: V_{CC}=±80V; for LS350: V_{CC}=±25V.
5. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

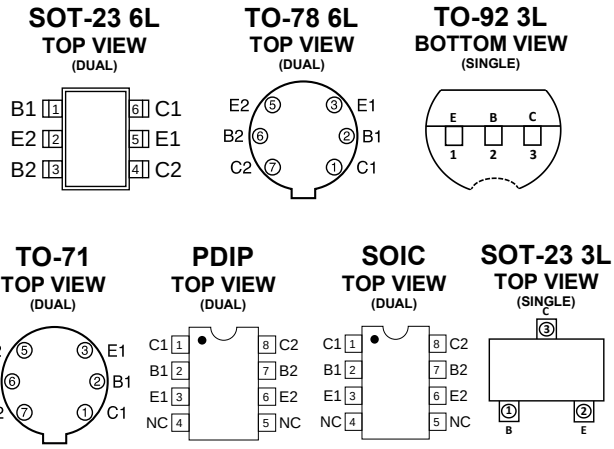
LINEAR SYSTEMS

Over Three Decades of Quality Through Innovation

LS3550 SERIES

MONOLITHIC DUAL & SINGLE PNP TRANSISTORS

FEATURES	
6 LEAD SOT-23 SURFACE MOUNT PACKAGE*	
TIGHT MATCHING[1]	2mV
EXCELLENT THERMAL TRACKING[1]	3µV/°C
ABSOLUTE MAXIMUM RATINGS[2] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Maximum Power Dissipation	
Continuous Power Dissipation	TBD
Maximum Currents	
Collector Current	50mA
Maximum Voltages	
Collector to Collector Voltage	60V



MATCHING ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated) * MATCHING ELECTRICAL CHARACTERISTICS FOR DUALS ONLY

SYMBOL	CHARACTERISTIC	LS3550A		LS3550B		LS3550C		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
$\lvert V_{BE1} - V_{BE2} \rvert$	Base to Emitter Voltage Differential		2		5		10	mV	I_C = -100µA, V_{CE} = -5V
$\frac{\lvert V_{BE1} - V_{BE2} \rvert}{\Delta T}$	Base to Emitter Voltage Differential Change with Temperature		3		5		15	µV/°C	I_C = -100µA, V_{CE} = -5V T_A = -40°C to +85°C
$\lvert I_{B1} - I_{B2} \rvert$	Base Current Differential		10		10		10	nA	I_C = -10µA, V_{CE} = -5V
$\frac{\lvert I_{B1} - I_{B2} \rvert}{\Delta T}$	Base Current Differential Change with Temperature		0.5		0.5		1.0	nA/°C	I_C = -10µA, V_{CE} = -5V T_A = -40°C to +85°C
h_{FE1}/h_{FE2}	Current Gain Differential		10		10		15	%	I_C = -1mA, V_{CE} = -5V

ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

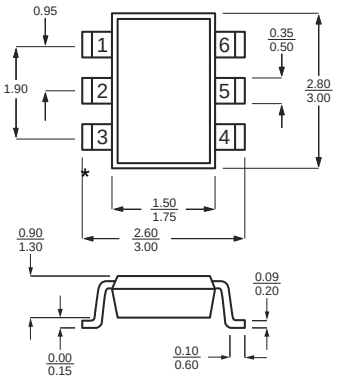
SYMBOL	CHARACTERISTIC	LS3550A		LS3550B		LS3550C		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
BV_{CBO}	Collector to Base Breakdown Voltage	-45		-40		-20		15	I_C = -10µA, I_E = 0A
BV_{CEO}	Collector to Emitter Breakdown Voltage	-45		-40		-20		16	I_C = -5mA, I_B = 0A
BV_{CCO}	Collector to Collector Breakdown Voltage	±60		±60		±60		V	I_{CC} = -±1µA, I_B=I_C =0A
BV_{EBO}	Emitter to Base Breakdown Voltage[3]	-6.0		-6.0		-6.0			I_E = -10µA, I_C = 0A
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage		-0.50		-0.50		-1.2		I_C = -10mA I_B = -1mA

ELECTRICAL CHARACTERISTICS CONT. @25 °C (unless otherwise stated)

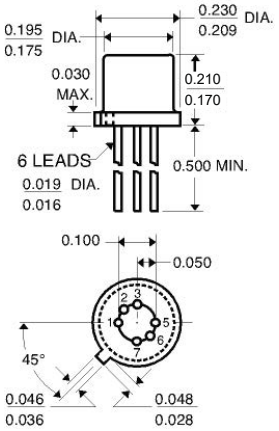
SYMBOL	CHARACTERISTIC	LS3550A		LS3550B		LS3550C		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	150		100		50			I_C = -1mA, V_{CE} = -5V
		120		80		40			I_C = -10mA, V_{CE} = -5V
		100		60		30			I_C = -35mA, V_{CE} = -5V
I_{CBO}	Collector Cutoff Current		-0.35		-0.35			nA	I_E = 0A, V_{CB} = -30V
							-0.35		I_E = 0A, V_{CB} = -20V
I_{EBO}	Emitter Cutoff Current		-0.35		-0.35		-0.35		I_E = 0A, V_{CB} = -3V
I_{C1C2}	Collector to Collector Leakage Current		±1		±1		±1	µA	V_{CC} = ±60V, I_B=I_C =0A
C_{OBO}	Output Capacitance		2		2		2	pF	I_E = 0A, V_{CB} = -10V
f_T	Gain Bandwidth Product (Current)		600		600		600	MHz	I_C = -1mA, V_{CE} = -5V
NF	Noise Figure (Narrow Band)		3		3		3	dB	I_C = -100µA, V_{CE} = -5V BW = 200Hz R_B = 10Ω, *f* = 1kHz

STANDARD PACKAGE DIMENSIONS:

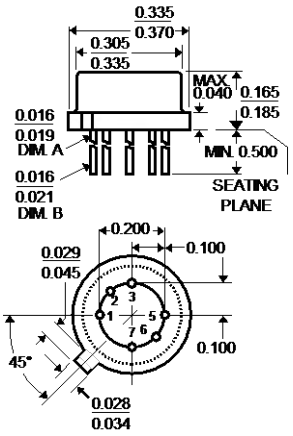
SOT-23 6L



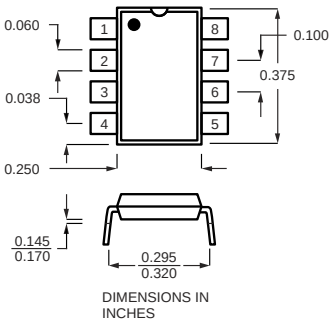
TO-71 6L



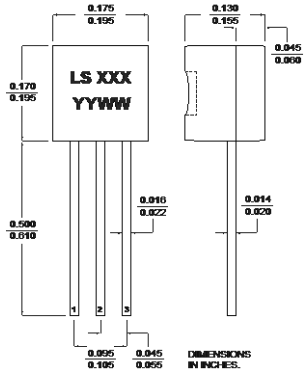
TO-78 6L



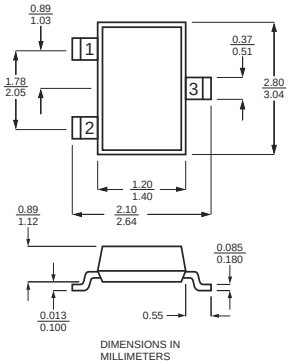
PDIP 8L



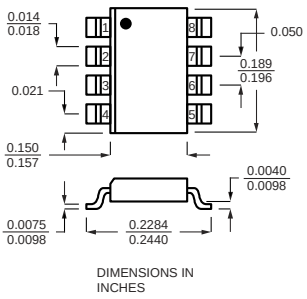
TO-92 3L



SOT-23 3L



SOIC 8L



NOTES:

1. Maximum rating for LS3550A, SOT-23-6L.
2. Absolute maximum ratings are limiting values above which serviceability may be impaired.
3. The reverse Base-to-Emitter voltage must never exceed -6.0 Volts. The reverse Base-to-Emitter current must never exceed -10µA.

LINEAR SYSTEMS

Improved Standard Products®

LS358

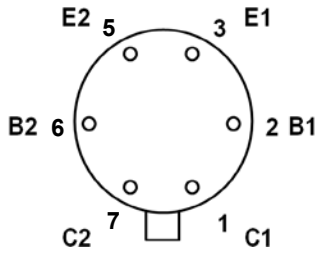
LOG CONFORMANCE MONOLITHIC DUAL PNP TRANSISTORS

FEATURES	
LOG CONFORMANCE	∆re ≤1Ω from ideal TYP.

ABSOLUTE MAXIMUM RATINGS NOTE 1 (T_A= 25°C unless otherwise noted)		
I_C	Collector-Current	-10mA

Maximum Temperatures	
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature	-55°C to +150°C

Maximum Power Dissipation	ONE SIDE	BOTH SIDES
Device Dissipation T_A=25°C	250mW	500mW
Linear Derating Factor	2.3mW/°C	4.3mW/°C



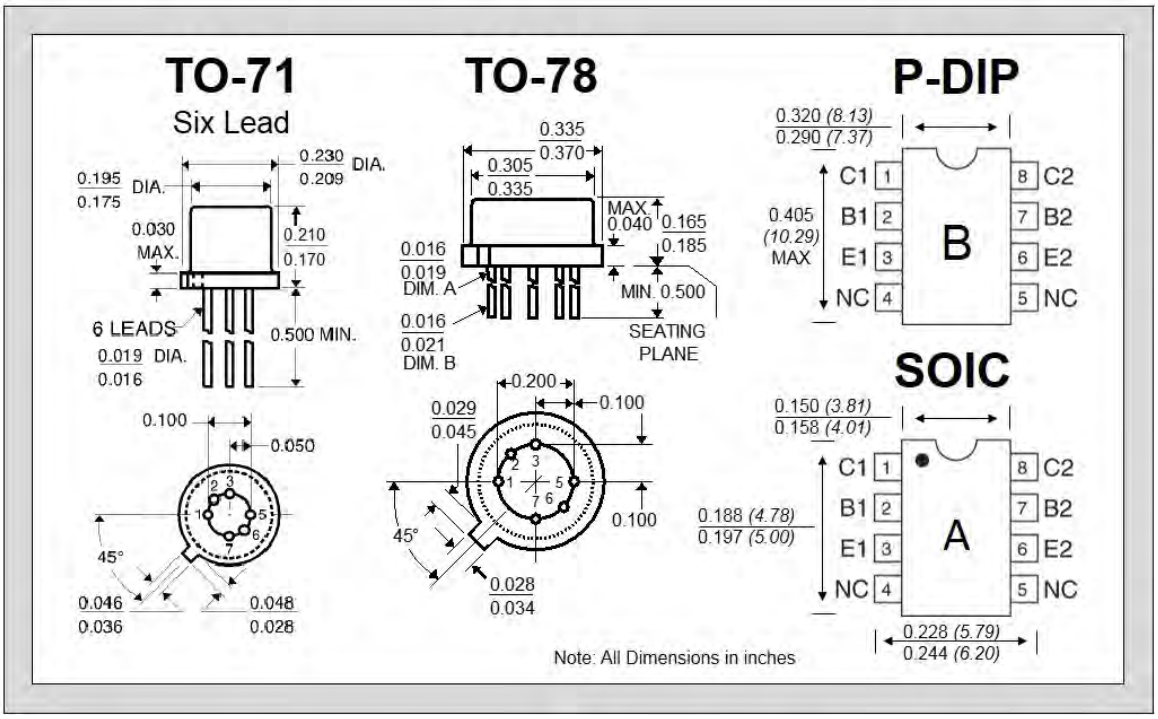
TO-71 & TO-78
TOP VIEW

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS358		UNITS	CONDITIONS	
∆re	Log Conformance	1.5		Ω	I_C = -10-100-1000µA	V_{CE} = -5V
BV_{CBO}	Collector-Base Breakdown Voltage	-20	MIN.	V	I_C = -10µA	I_E = 0A
BV_{CEO}	Collector to Emitter Voltage	-20	MIN.	V	I_C = -1mA	I_B = 0A
BV_{EBO}	Emitter-Base Breakdown Voltage	-6.0	MIN.	V	I_E = -10µA	I_C = 0A **NOTE 2**
BV_{CCO}	Collector to Collector Voltage	45	MIN.	V	I_C = ±10µA, I_B=I_E = 0A	
h_{FE}	DC Current Gain	100 600	MIN. MAX.		I_C = -10µA	V_{CE} = -5V
h_{FE}	DC Current Gain	100 600	MIN. MAX.		I_C = -100µA	V_{CE} = -5V
h_{FE}	DC Current Gain	100	MIN.		I_C = -1mA	V_{CE} = -5V
V_{CE}(SAT)	Collector Saturation Voltage	-0.5	MAX.	V	I_C = -1mA	I_B = -0.1mA
I_{CBO}	Collector Cutoff Current	-0.2	MAX.	nA	I_E = 0A	V_{CB} = -15V
I_{EBO}	Emitter Cutoff Current	-0.2	MAX.	nA	I_C = 0A	V_{EB} = -3V
C_{OBO}	Output Capacitance[4]	2.0	MAX.	pF	I_E = 0A	V_{CB} = -5V
C_{C1C2}	Collector to Collector Capacitance[4]	2.0	MAX.	pF	V_{CC} = 0V	
I_{C1C2}	Collector to Collector Leakage Current	±0.5	MAX.	µA	V_{CC} = ±45V	I_B = I_E = 0A
f_T	Current Gain Bandwidth Product[4]	200	MIN.	MHz	I_C = -1mA	V_{CE} = -5V
NF	Narrow Band Noise Figure[4]	3.0	MAX.	dB	I_C = -100µA BW = 200Hz f=1KHz	V_{CE} = -5V R_G = 10 KΩ

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS358		UNITS	CONDITIONS
$\lvert V_{BE1}-V_{BE2}\rvert$	Base Emitter Voltage Differential	0.4 1	TYP. MAX.	mV mV	I_C = -10 µA V_{CE} = -5V
$\Delta\lvert (V_{BE1}-V_{BE2})\rvert$/°C	Base Emitter Voltage Differential[4] Change with Temperature	1	TYP.	µV/°C	I_C = -10 µA V_{CE} = -5V T_A = -55°C to +125°C
$\lvert I_{B1}-I_{B2}\rvert$	Base Current Differential	5	MAX.	nA	I_C = -10 µA V_{CE} = -5V
$\lvert \Delta (I_{B1}-I_{B2})\rvert$/°C	Base Current Differential[4] Change with Temperature	0.5	TYP.	nA/°C	I_C = -10 µA V_{CE} = -5V T_A = -55°C to +125°C
h_{FE1}/h_{FE2}	DC Current Gain Differential	5	TYP.	%	I_C = -10 µA V_{CE} = -5V



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. The reverse base-to-emitter voltage must never exceed 6.0 volts; the reverse base-to-emitter current must never exceed 10 µA.
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate electrical polarity only.
4. Not tested; guaranteed by design.

LINEAR SYSTEMS

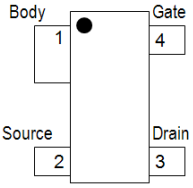
Improved Standard Products®

3N170 3N171

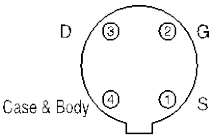
N-CHANNEL MOSFET ENHANCEMENT MODE

FEATURES	
Direct Replacement for INTERSIL 3N170 & 3N171	
LOW DRAIN TO SOURCE RESISTANCE	$r_{ds(on)} \leq 200\Omega$
FAST SWITCHING	$t_{d(on)} \leq 3.0$ns
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150 °C
Operating Junction Temperature	-55 to +135 °C
Maximum Power Dissipation	
Continuous Power Dissipation	300mW
Maximum Current	
Drain to Source	30mA
Maximum Voltages	
Drain to Gate	±35V
Drain to Source	25V
Gate to Source	±35V

3N170 & 3N171
SOT-143 4L
Top View



3N170 & 3N171
TO-72 4L
Top View



ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated) (V_{SB} = 0V unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_{DSS}	Drain to Source Breakdown Voltage		25			V	I_D = 10µA, V_{GS} = 0V
$V_{DS(on)}$	Drain to Source "On" Voltage				2.0		I_D = 10mA, V_{GS} = 10V
$V_{GS(th)}$	Gate to Source Threshold Voltage	3N170	1.0		2.0		V_{DS} = 10V, I_D = 10µA
		3N171	1.5		3.0		
I_{GSS}	Gate Leakage Current				10	pA	V_{GS} = -35V, V_{DS} = 0V
I_{DSS}	Drain Leakage Current "Off"				10	nA	V_{DS} = 10V, V_{GS} = 0V
$I_{D(on)}$	Drain Current "On"		10			mA	V_{GS} = 10V, V_{DS} = 10V
g_{fs}	Forward Transconductance		1000			µS	V_{DS} = 10V, I_D = 2.0mA, *f* = 1.0kHz
$r_{ds(on)}$	Drain to Source "On" Resistance				200	Ω	V_{GS} = 10V, I_D = 100µA, *f* = 1.0kHz
C_{rss}	Reverse Transfer Capacitance				1.3	pF	V_{DS} = 0V, V_{GS} = 0V, *f* = 1.0MHz
C_{iss}	Input Capacitance				5.0		V_{DS} = 10V, V_{GS} = 0V, *f* = 1.0MHz
C_{db}	Drain to Body Capacitance				5.0		V_{DB} = 10V, *f* = 1.0MHz

SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$t_{d(on)}$	Turn On Delay Time			3.0	ns	V_{DD} = 10V, $ID_{D(on)}$ = 10mA, $V_{GS(on)}$ = 10V, $V_{GS(off)}$ = 0V R_G = 50Ω
t_r	Turn On Rise Time			10		
$t_{d(off)}$	Turn Off Delay Time			3.0		
t_f	Turn Off Fall Time			15		

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.

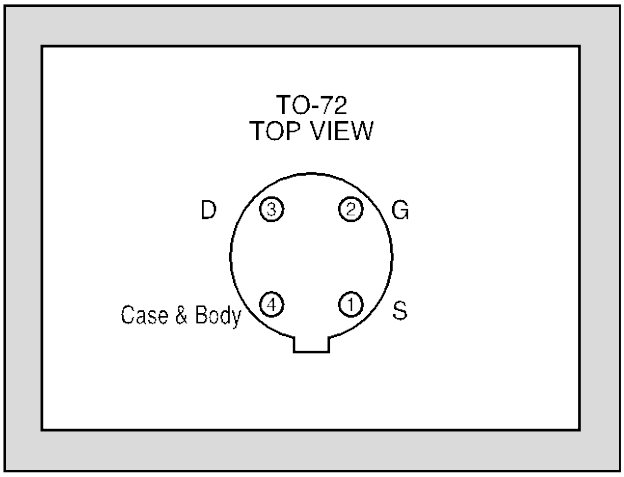
LINEAR SYSTEMS

Improved Standard Products®

2N4351

N-CHANNEL MOSFET ENHANCEMENT MODE

FEATURES	
DIRECT REPLACEMENT FOR INTERSIL 2N4351	
HIGH DRAIN CURRENT	I_D = 20mA
HIGH GAIN	g_{fs} = 1000µS
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Maximum Power Dissipation, T_A=25°C	
Continuous Power Dissipation[3]	350mW
Maximum Current	
Drain to Source	20mA
Maximum Voltages	
Drain to Body	25V
Drain to Source	25V
Gate to Source	±30V

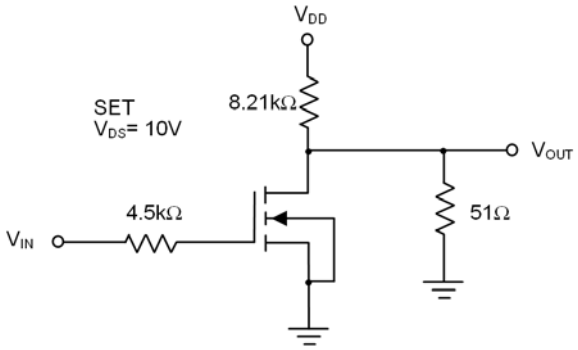


ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated) (V_{SB} = 0V unless otherwise stated)

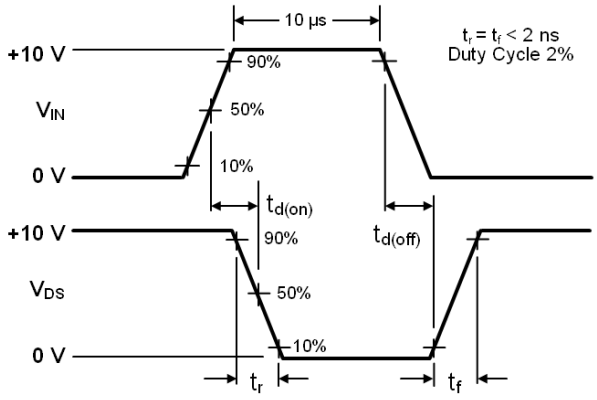
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{DSS}	Drain to Source Breakdown Voltage	25			V	I_D = 10µA, V_{GS} = 0V
$V_{DS(on)}$	Drain to Source "On" Voltage			1		I_D = 2mA, V_{GS} = 10V
$V_{GS(th)}$	Gate to Source Threshold Voltage	1		5		V_{DS} = 10V, I_D = 10µA
I_{GSS}	Gate Leakage Current			±10	pA	V_{GS} = ±30V, V_{DS} = 0V
I_{DSS}	Drain Leakage Current "Off"			10	nA	V_{DS} = 10V, V_{GS} = 0V
$I_{D(on)}$	Drain Current "On"	3			mA	V_{GS} = 10V, V_{DS} = 10V
g_{fs}	Forward Transconductance	1000			µS	V_{DS} = 10V, I_D = 2mA, *f* = 1kHz
$r_{ds(on)}$	Drain to Source "On" Resistance			300	Ω	V_{GS} = 10V, I_D = 100uA, *f* = 1kHz
C_{rss}	Reverse Transfer Capacitance[2]			1.3	pF	V_{DS} = 0V, V_{GS} = 0V, *f* = 140kHz
C_{iss}	Input Capacitance[2]			5.0		V_{DS} = 10V, V_{GS} = 0V, *f* = 140kHz
C_{db}	Drain to Body Capacitance[2]			5.0		V_{DB} = 10V, *f* = 140kHz

SYMBOL	CHARACTERISTIC	MAX	UNITS
$t_{d(on)}$	Turn On Delay Time[2]	45	ns
t_r	Turn On Rise Time[2]	65	
$t_{d(off)}$	Turn Off Delay Time[2]	60	
t_f	Turn Off Fall Time[2]	100	

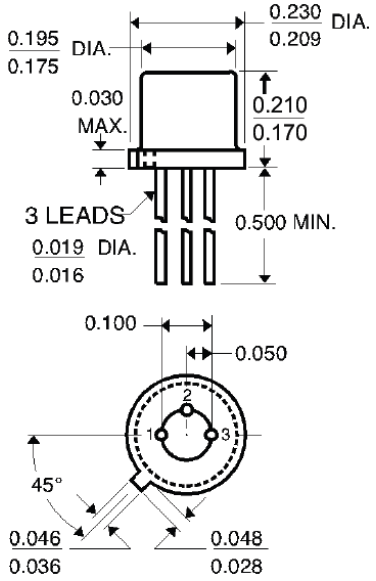
SWITCHING TEST CIRCUIT



TIMING WAVEFORMS



TO-72
4 LEAD



DIMENSIONS IN INCHES

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.

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2. Not a production test. Guaranteed by design.
3. Derate 2.8 mW ºC above 25 ºC.

LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

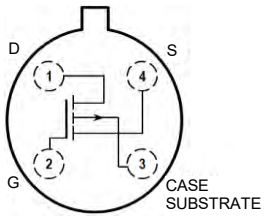
3N163 and 3N164

P-Channel Enhancement Mode MOSFET

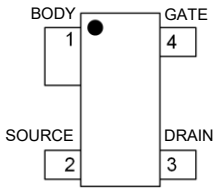
VERY HIGH INPUT IMPEDANCE, HIGH GATE BREAKDOWN, FAST SWITCHING, LOW CAPACITANCE

FEATURES	
VERY HIGH INPUT IMPEDANCE	
HIGH GATE BREAKDOWN	
ULTRA LOW LEAKAGE	
FAST SWITCHING	
LOW CAPACITANCE	
ABSOLUTE MAXIMUM RATINGS	
@ 25°C (unless otherwise stated)	
Drain-Source or Drain-Gate Voltage	
3N163	-40V
3N164	-30V
Drain Current	50mA
Storage Temperature	-55ºC to +150ºC
Power Dissipation TO-72 case	375mW[2]
Power Dissipation SOT-143 case	350mW[3]

TO-72 4L
TOP VIEW



SOT-143 4L
TOP VIEW



TO-72 4L
PACKAGE
PHOTO

SOT-143 4L
TOP VIEW

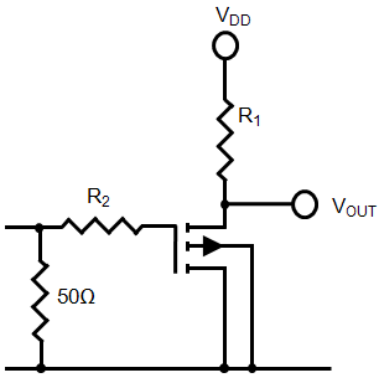
ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	3N163		3N164		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
I_{GSS}	Gate Leakage Current		-10		-10	pA	V_{GS}=-40V, V_{DS}=0 (3N163), V_{SB}=0V
	T_A=+125ºC		-25		-25		V_{GS}=-30V, V_{DS}=0 (3N164), V_{SB}=0V
BV_{DSS}	Drain-Source Breakdown Voltage	-40		-30			I_D=-10µA V_{GS}=0, V_{BS}=0
BV_{SDS}	Source-Drain Breakdown Voltage	-40		-30		V	I_S=-10µA V_{GD}=0, V_{BD}=0
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0		V_{DS}=V_{GS} I_D=-10µA, V_{SB}=0V
V_{GS}	Gate Source Voltage (on)	-3.0	-6.5	-3.0	-6.5		V_{DS}=-15V I_D=-0.5mA, V_{SB}=0V
I_{DSS}	Zero Gate Voltage, Drain Current (off)		-200		-400	pA	V_{DS}=-15V V_{GS}=0, V_{SB}=0V
I_{SDS}	Zero Gate Voltage, Source Current		-400		-800		V_{SD}=-15V V_{GS}=0, V_{DB}=0V
$R_{DS(on)}$	Drain-Source on Resistance		250		300	ohms	V_{GS}=-20V I_D=-100µA, V_{SB}=0V
$I_{D(on)}$	On Drain Current	-5.0	-30	-3.0	-30	mA	V_{DS}=-15V V_{GS}=-10V, V_{SB}=0V
g_{fs}	Forward Transconductance	2.0	4.0	1.0	4.0	mS	V_{DS}=-15V I_D=-10mA f=1kHz
g_{og}	Output Admittance		250		250	µS	
C_{iss}	Input Capacitance-Output Shorted		3.5		3.5	pF	V_{DS}=-15V I_D=-10mA [1] f=1MHz
C_{rss}	Reverse Transfer Capacitance		0.7		0.7		
C_{oss}	Output Capacitance Input Shorted		3.0		3.0		

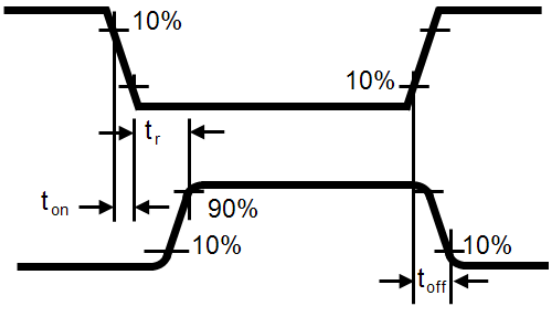
SWITCHING CHARACTERISTICS T_A=25°C and V_{BS}=0 (unless otherwise noted)

SYMBOL	CHARACTERISTIC	3N163		3N164		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
t_{on}	Turn-On Delay Time		12		12	ns	V_{DD}=-15V, V_{SB}=0V $I_{D(on)}$=-10mA[1] R_G=R_L=1.4K
t_r	Rise Time		24		24		
t_{off}	Turn-Off Time		50		50		

Switching Times Test Circuit



TYPICAL SWITCHING WAVEFORM

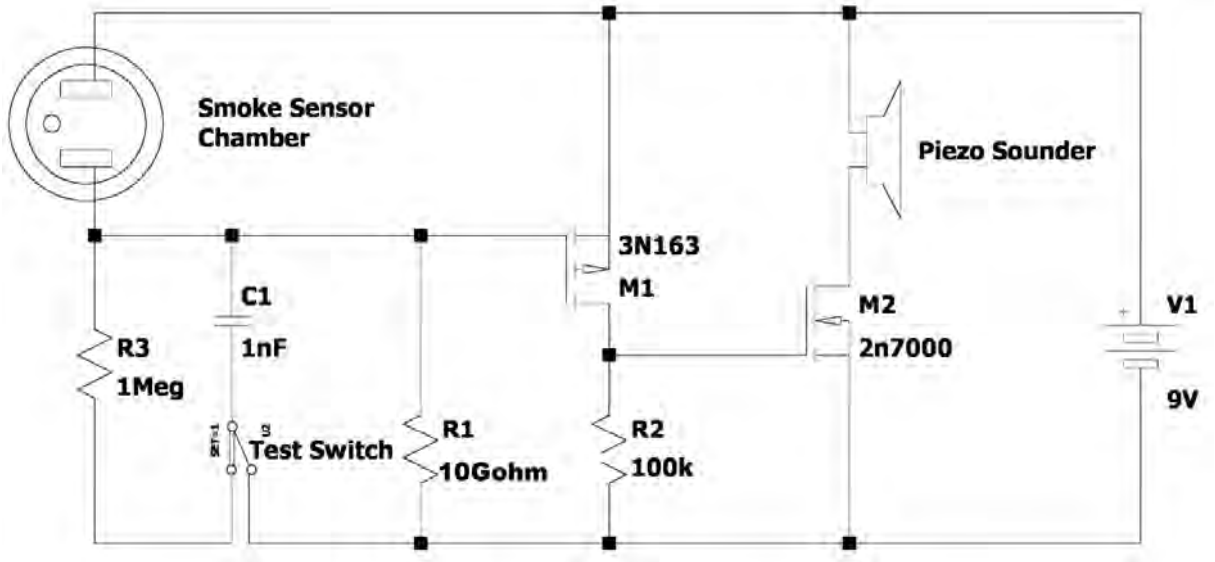


INPUT PULSE
Rise Time≤2ns
Pulse Width≥200ns

SAMPLING SCOPE
T_r≤0.2ns
C_{IN}≤2pF
R_{IN}≥10M

Simplest Possible Smoke Detector

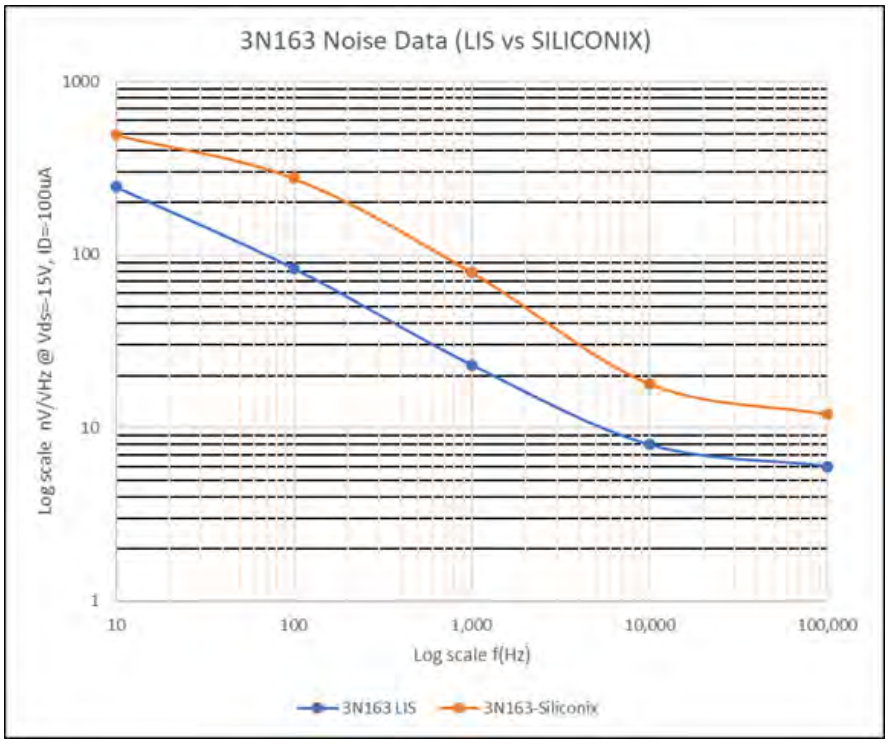
KRL 09/26/2021



NOTES:

1. For design reference only, not 100% tested.
2. Derate 3mW/ºC above 25ºC
3. Derate 3.5mW/ºC above 25ºC
4. All min/max limits are absolute numbers. Negative signs indicate electrical polarity only.

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



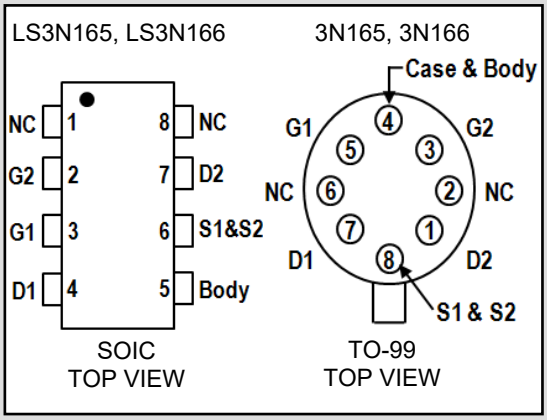
LINEAR SYSTEMS

Improved Standard Products®

3N/LS165, 3N/LS166

MONOLITHIC DUAL P-CHANNEL ENHANCEMENT MODE MOSFET

FEATURES	
VERY HIGH INPUT IMPEDANCE	
HIGH GATE BREAKDOWN	
ULTRA LOW LEAKAGE	
LOW CAPACITANCE	
ABSOLUTE MAXIMUM RATINGS (NOTE 1) (T_A=25°C unless otherwise noted)	
Drain-Source or Drain-Gate Voltage **(NOTE 2)**	
3N165	40 V
3N166	30 V
Gate-Gate Voltage	±80 V
Drain Current **(NOTE 2)**	50 mA
Storage Temperature	-55ºC to +150ºC
Operating Temperature	-55ºC to +150ºC
Lead Temperature (Soldering, 10 sec.)	+300ºC
Power Dissipation (One Side)	300 mW
Total Derating above 25ºC	4.2 mW/ºC

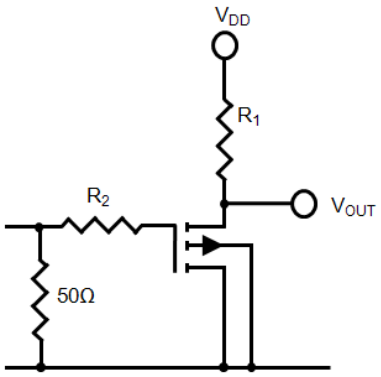


ELECTRICAL CHARACTERISTICS (T_A=25°C and V_{BS}=0 unless otherwise noted)

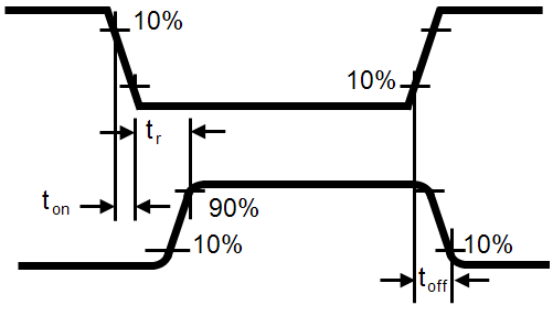
SYMBOL	CHARACTERISTIC	3N165 & 3N166 MIN	3N165 & 3N166 MAX	LS3N165 & LS3N166 MIN	LS3N165 & LS3N166 MAX	UNITS	CONDITIONS
I_{GSSR}	Gate Reverse Leakage Current	--	10	--	100	pA	V_{GS}=40V
I_{GSSF}	Gate Forward Leakage Current	--	-10	--	-100	pA	V_{GS}=-40V
		--	-25	--	--	pA	T_A=+125ºC
I_{DSS}	Drain to Source Leakage Current	--	-200		-200	pA	V_{DS}=-20 V, V_{GS}=V_{BS}=0V
I_{SDS}	Source to Drain Leakage Current	--	-400	--	-400	pA	V_{SD}=-20 V, V_{GD}=V_{DB}=0V
$I_{D(on)}$	On Drain Current	-5	-30	-5	-30	mA	V_{DS}=-15V V_{GS}=-10 V V_{SB}=0V
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	-2	-5	V	V_{DS}=-15V I_D=-10µA V_{SB}=0V
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	-2	-5	V	V_{DS}=V_{GS} I_D=-10µA V_{SB}=0V
$r_{DS(on)}$	Drain Source ON Resistance	--	300	--	300	ohms	V_{GS}=-20V I_D=-100µA V_{SB}=0V
g_{fs}	Forward Transconductance	1500	3000	1500	3000	µS	V_{DS}=-15V I_D=-10mA f=1kHz
g_{os}	Output Admittance	--	300	--	300	µS	V_{SB}=0V
C_{lss}	Input Capacitance	--	3.0	--	3.0	pF	
C_{rss}	Reverse Transfer Capacitance	--	0.7	--	1.0	pF	V_{DS}=-15V I_D=-10mA f=1MHz
C_{oss}	Output Capacitance	--	3.0	--	3.0	pF	**(NOTE 3)** V_{SB}=0V
$R_E(Y_{ls})$	Common Source Forward Transconductance	1200	--			µS	V_{DS}=-15V I_D=-10mA f=100MHz **(NOTE 3)** V_{SB}=0V

MATCHING CHARACTERISTICS 3N165

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS
G_{fs1}/G_{fs2}	Forward Transconductance Ratio	0.90	1.0		V_{DS}=-15V I_D=-500 µA f=1kHz V_{SB}=0V
V_{GS1-2}	Gate Source Threshold Voltage Differential	--	100	mV	V_{DS}=-15V I_D=-500 µA V_{SB}=0V
$\Delta V_{GS1-2}/\Delta T$	Gate Source Threshold Voltage Differential Change with Temperature	--	100	µV/ºC	V_{DS}=-15V I_D=-500 µA V_{SB}=0V T_A=-55ºC to = +125ºC



TYPICAL SWITCHING WAVEFORM



INPUT PULSE
Rise Time≤2ns
Pulse Width≥200ns

SAMPLING SCOPE
T_r≤0.2ns
C_{IN}≤2pF
R_{IN}≥10M

Typical Switching Time Test Circuit

NOTES:

1. MOS field effect transistors have extremely high input resistance and can be damaged by the accumulation of excess static charge. To avoid possible damage to the device while wiring, testing, or in actual operation, follow these procedures:
   To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used. Avoid unnecessary handling. Pick up devices by the case instead of the leads. Do not insert or remove devices from circuits with the power on, as transient voltages may cause permanent damage to the devices.
2. Per transistor.
3. For design reference only, not 100% tested.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3N190/3N191

Dual P-Channel Enhancement Mode MOSFET

LOW TOTAL HARMONIC DISTORTION (THD) AND VOLTAGE NOISE MOSFET

FEATURES	
DIRECT REPLACEMENT FOR INTERSIL 3N190 & 3N191	
LOW GATE LEAKAGE CURRENT	I_{GSS} ≤ ±10pA
LOW TRANSFER CAPACITANCE	C_{rss} ≤ 1.0pF
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150 °C
Operating Junction Temperature	-55 to +135 °C
Maximum Power Dissipation @ TA=25ºC	
Continuous Power Dissipation One Side	300mW
Continuous Power Dissipation Both Sides	525mW
Maximum Current	
Drain to Source[2]	30mA
Maximum Voltages	
Drain to Gate[2]	40V
Drain to Source[2]	40V
Gate to Gate	±60V

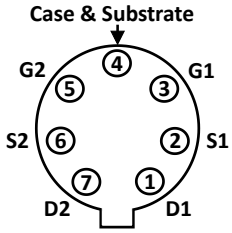
Package Photo

TO-78 7L

Side View

Pin Configuration

TO-78 7L



Top View

Features

- Very High Input Impedance
- High Gate Breakdown
- Low Capacitance
- High Switching Frequency

Benefits

- Minimal Response Time.
- Generates less heat loss compared to BJT at high currents.
- Great at amplifying analog signals.
- Reduces design complexity in medium and low power applications.
- Ideal Choice for high-side switches.
- Simplified gate driving technique reduces overall cost.

Applications

- Switching Applications
- Amplifying Circuits
- Chopper Circuits
- High-Frequency Amplifier
- Voltage Regulator Circuits
- Inverter
- DC Brushless Motor Drives
- DC Relay
- Digital Circuits

Description

The 3N190/3N191 Series is a Dual, P-Channel, Enhancement Mode MOSFET. The MOSFET is a voltage controlled solid state device. The simplicity of the design is advantageous for non-isolated POL(Point of Load) power supplies and low-voltage drives applications, where space is limited. The simplified gate driving technique is often a beneficial characteristic for designers because it reduces overall cost. The 3N190/3N191 Series has a very high switching frequency so that they are used in high-speed load switching, given their minimal response time. The 3N190/3N191 can be used for digital control of higher current and higher voltage loads than the ratings that a microcontroller can withstand. They are great at amplifying analog signals, especially in audio applications. They have multiple functions in different types of applications and can also be used as a chopper or regulator. The 3N190 and 3N191 are the same products as a second source for Intersil products.

MATCHING CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
g_{fs1}/g_{fs2}	Forward Transconductance Ratio	0.85	-	1.0	-	V_{DS} = -15V, I_D = -500µA, *f* = 1kHz
V_{GS1-2}	Gate to Source Threshold Voltage Differential	-	-	100	mV	V_{DS} = -15V, I_D = -500µA
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate to Source Threshold Voltage Differential with Temperature[4]	-	50	-	µV/°C	V_{DS} = -15V, I_D = -500µA T_S = -55 to +25 °C
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate to Source Threshold Voltage Differential with Temperature[4]	-	50	-		V_{DS} = -15V, I_D = -500µA T_S = +25 to +125 °C

ELECTRICAL CHARACTERISTICS @ 25 °C

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{DSS}	Drain to Source Breakdown Voltage	-40	-	-	V	I_D = -10µA
BV_{SDS}	Source to Drain Breakdown Voltage	-40	-	-		I_S = -10µA, V_{BD} = 0V
V_{GS}	Gate to Source Voltage	-3.0	-	-6.5		V_{DS} = -15V, I_D = -500µA
$V_{GS(th)}$	Gate to Source Threshold Voltage	-2.0	-	-5.0		V_{DS} = V_{GS}, I_D = -10µA
		-2.0	-	-5.0		V_{DS} = -15V, I_D = -500µA
I_{GSSR}	Reverse Gate Leakage Current	-	-	10	pA	V_{GS} = 40V
I_{GSSF}	Forward Gate Leakage Current	-	-	-10		V_{GS} = -40V
I_{DSS}	Drain Leakage Current "Off"	-	-	-200		V_{DS} = -15V
I_{SDS}	Source to Drain Leakage Current "Off"	-	-	-400		V_{SD} = -15V, V_{DB} = 0V
$I_{D(on)}$	Drain Current[2]	-5.0	-	-30.0	mA	V_{DS} = -15V, V_{GS} = -10V
I_{G1G2}	Gate to Gate Isolation Current	-	-	±1.0	µA	V_{G1G2} = ±80V, I_D = I_S = 0 = mA
g_{fs}	Forward Transconductance[4]	1500	-	4000	µS	V_{DS} = -15V, I_D = -5mA, *f* = 1kHz
g_{os}	Output Admittance	-	-	300		
$r_{ds(on)}$	Drain to Source "On" Resistance	-	-	300	Ω	V_{DS} = -20V, I_D = -100µA
C_{rss}[3]	Reverse Transfer Capacitance	-	-	1.0	pF	V_{DS} = -15V, I_D = -5mA, *f* = 1MHz
C_{iss}[3]	Input Capacitance Output Shorted	-	-	4.5		
C_{oss}[3]	Output Capacitance Input Shorted	-	-	3.0		

3N190/191 P-CHANNEL ENHANCEMENT MODE MOSFET

TO-78 7L Substrate (Case) Pin-4 Biasing Recommendation

In order to improve the overall product performance, we strongly recommend Substrate (Case) pin to be connected to highest VCC potential at Pin-4 with an optional 10KΩ resistor. This ensures strong reverse biasing of junction isolation diode and resulting improvement in Total Harmonic Distortion (THD) and Voltage Noise (Vn) performances. This applied voltage must be maximum 38V which is 2.0V less than device BVDSS breakdown voltage of 40V-max.

SWITCHING CHARACTERISTICS

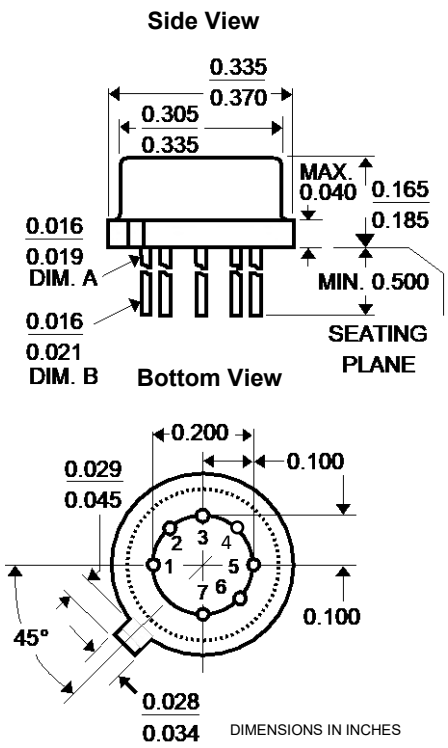
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$t_{d(on)}$[3]	Turn On Delay Time	-	-	15	ns	V_{DD} = -15V, $I_{D(on)}$ = -5mA,
t_r[3]	Turn On Rise Time	-	-	30		R_G = R_L = 1.4kΩ
t_{off}[3]	Turn Off Time	-	-	50		

Notes

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Per Transistor.
3. For design reference only. Not 100% tested.
4. Measured at end points, T_A and T_B.
5. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

Package Dimensions

TO-78 7 Lead



Ordering Information

Standard Part Call-Out
3N190 TO-78 7L RoHS
3N191 TO-78 7L RoHS
Custom Part Call-Out (Custom Parts Include SEL + 4 Digit Numeric Code)
3N190 TO-78 7L RoHS SELXXXX
3N191 TO-78 7L RoHS SELXXXX

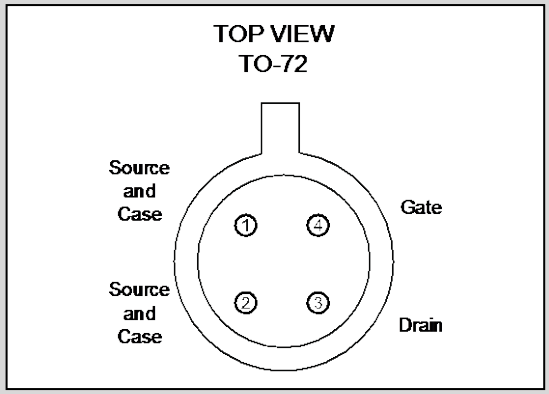
LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

LS320

HIGH INPUT IMPEDANCE BIFET AMPLIFIER

FEATURES	
HIGH INPUT IMPEDANCE	r_{Gs} = 100GΩ
HIGH TRANSCONDUCTANCE	Y_{FS} = 30,000µS
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +125 °C
Maximum Power Dissipation	
Continuous Power Dissipation @ +25 °C	200mW
Maximum Currents	
Drain Current	I_D = 25mA
Maximum Voltages	
Drain to Source[1]	V_{DSO} = 20V
Gate to Source	V_{GSS} = 20V



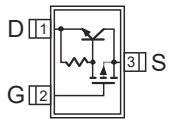
ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
V_{DS}	Drain to Source Voltage	-20			V	I_{DS} = 100µA, V_{GS} = 0V
V_{GS}	Gate to Source Voltage	-7	-10	-12	V	I_{DS} = 10mA, V_{DS} = -10V[2,3]
g_{fs}	Common Source Forward Transconductance	30,000			µS	I_{DS} = 10mA, V_{DS} = -10V, *f* = 1kHz
g_{oss}	Common Source Output Conductance		300		µS	I_{DS} = 10mA, V_{DS} = -10V, *f* = 1kHz
r_{Gs}	Gate to Source Input Resistance	100			GΩ	V_{GS} = 0 to 20V, T_J to 125 °C
C_{ISS}	Input Capacitance		8		pF	I_{DS} = 10mA, V_{DS} = -10V
C_{RSS}	Reverse Transfer Capacitance		1.5		pF	I_{DS} = 10mA, V_{DS} = -10V
e_n	Noise Voltage		25		µV	I_{DS} = 10mA, V_{DS} = 10V BW = 50 to 15kHz

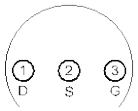
All limits are absolute numbers. Negative signs indicate electrical polarity.

PACKAGE OPTIONS

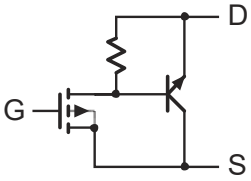
SOT-23
TOP VIEW



TO-92
TOP VIEW



FUNCTIONAL



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. The gate to source voltage must never exceed 100V, t < 10ms.
3. Additional screening available

LINEAR SYSTEMS

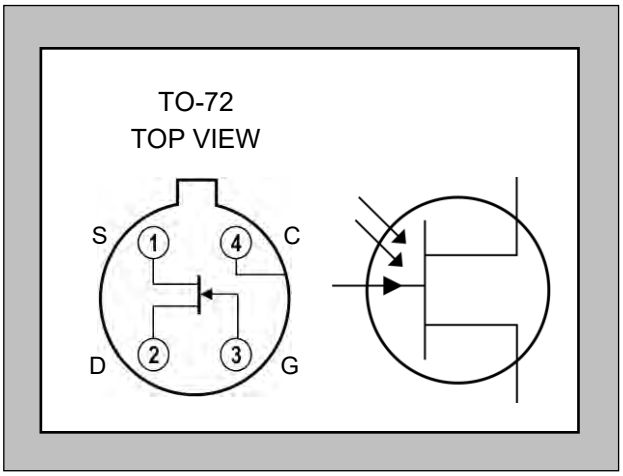
Over 30 Years of Quality Through Innovation

LS627

PHOTO FET
LIGHT SENSITIVE JFET

FEATURES
DIRECT REPLACEMENT FOR CRYSTALONICS FF627
FLAT GLASS TOP FOR EXTERNAL OPTICS
ULTRA HIGH SENSITIVITY

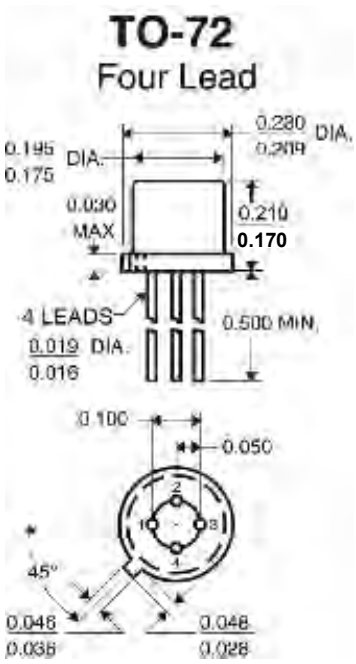
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +200 °C
Operating Junction Temperature	-55 to +165 °C
Maximum Power Dissipation	
Continuous Power Dissipation, T_A=25°C	400mW
Maximum Currents	
Drain to Source	50mA
Maximum Voltages	
Drain to Gate	15V
Drain to Source	15V
Gate to Source	-10V



ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$V_{GS(off)}$	Gate to Source cutoff Voltage (V_{PO})	1.0		5.0	V	V_{DS} = 10V, I_D = 0.1µA
S_G	Gate Sensitivity[2, 7]	6.4		24	µA/mW/cm²	V_{DS} = 10V, V_{GS} = 0V, λ = 0.9µm
S_D	Drain Sensitivity[3, 7]		500		mA/mW/cm²	V_{DS} = 10V, V_{GS} = 0V, R_G = 1MΩ
λ_{Ig}	Gate Current (Light)[4, 7]	10		37.5	nA/FC	V_{DS} = 10V, V_{GS} = 0V
λ_{Id}	Drain Current (Light)[4, 7]		800		µA/FC	V_{DS} = 10V, V_{GS} = 0V, R_G = 1MΩ
I_{DSS}	Drain Saturation Current	8.0			mA	V_{DS} = 10V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current (Dark)			30	pA	V_{GS} = -10V, V_{DS} = 0V
g_{fs}	Forward Transconductance (g_m)	8000			µS	V_{DS} = 10V, V_{GS} = 0V, *f* = 1kHz
$R_{DS(on)}$	Drain to Source On Resistance		100		Ω	V_{DS} = 0.1V, V_{GS} = 0V
C_{GS}	Gate to Source Capacitance[7]			35	pF	V_{GS} = -10V, *f* = 140kHz
C_{GD}	Gate to Drain Capacitance[7]			20		V_{GD} = -10V, *f* = 140kHz
t_r	Rise Time[5, 7]		30		ns	V_{DS} = 10V, R_L = R_G =100Ω
t_f	Fall Time[6, 7]		50			

STANDARD PACKAGE DIMENSIONS:



Dimensions in inches

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Gate Current per unit Radient Power Density at Lens Surface
3. Drain Current per unit Radient Power Density (λ = 0.9µm).
4. Tungsten Lamp 2800°K Color Temperature.
5. GaAs Diode Source.
6. Directly Proportional to R_G.
7. Not production tested. Guaranteed by design.

LINEAR SYSTEMS

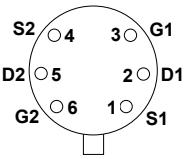
Improved Standard Products®

VCR11N

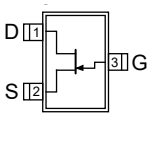
N-Channel JFET, Voltage Controlled Resistor

Simplify your Gain Control and Attenuation Designs Using Fewer Parts

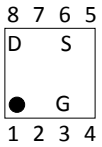
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150°C
Junction Operating Temperature	-55 to +135°C
Maximum Power Dissipation	
Continuous Power Dissipation @ Ta= +25°C	300mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = -25V
Gate to Drain	V_{GDS} = -25V



TO-71 6L
Top View



SOT-23 6L
Top View



DFN 8L
Top View

Features

- Continuous Voltage-Controlled Resistance
- High Off-Isolation
- High Input Impedance
- Gain Ranging Capability
- Simplified Drive Voltage Capabilities
- No Circuit Interaction
- Wide Range Signal Attenuation
- Pin-for-Pin Replacement for Siliconix VCR11N

Benefits

- Wide Range Signal Attenuation
- Gain Ranging
- Simplified Gate Drive
- High Breakdown Voltage
- No Circuit Interaction

Applications

- Amplifier Gain Control
- Oscillator Amplitude Control
- Small Signal Attenuations
- Filters

Description

A voltage-controlled resistor (VCR) is a three-terminal variable resistor where the resistance value between two of the terminals is controlled by a voltage potential applied to the third. The VCR is capable of operation as a symmetrical resistor with no dc bias voltage in the signal loop, an ideal characteristic for many applications.

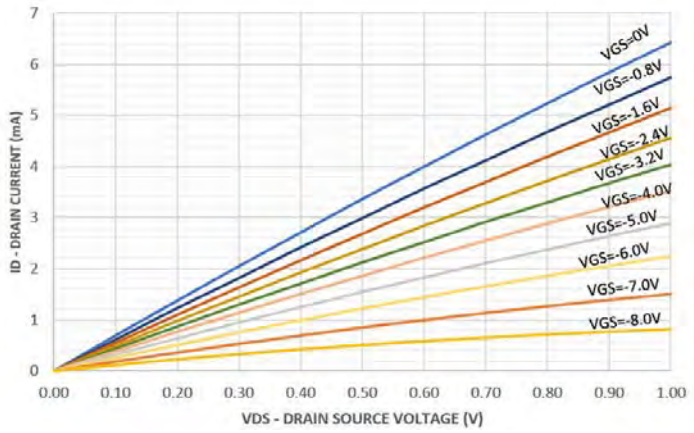
The VCR11N is specially intended for applications where the drain-source voltage is a low-level AC signal with no DC component. The key device performance is the predictable RDS change with no change in V_{GS} voltage. The VCR11N is available in the TO-71 6 lead package.

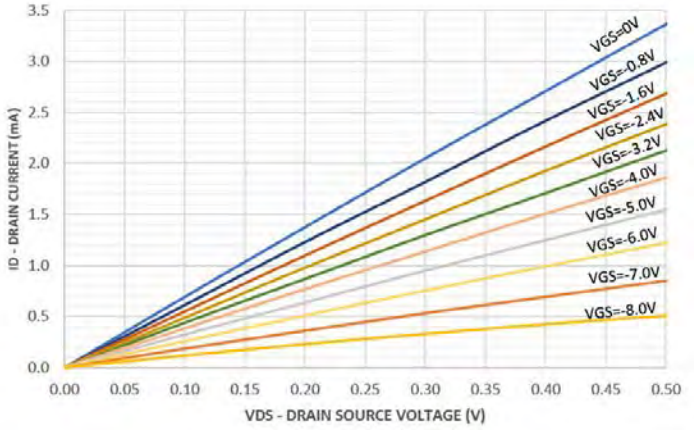
Electrical Characteristics @ Tj= 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-25			V	I_G = -1µA, V_{DS} = 0V
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-8		-12	V	I_D = 1µA, V_{DS} 10V
I_{GSS}	Gate to Source Leakage Current			-0.2	nA	V_{GS} = -15V, V_{DS} = 0V
$r_{DS(on)}$	Dynamic Drain to Source "ON" Resistance	100		200	Ω	V_{GS} =0V, I_D=500µA
		100		200	Ω	V_{GS} =0V, I_D=1mA
r_{DS1}/r_{DS2}	Static Drain to Source "ON" Resistance Ratios	0.95		1		V_{GS} =0V, I_D=500µA
		0.95		1		V_{GS} =0V, I_D=1mA
C_{dgo}	Drain to Gate Capacitance			8	pF	V_{GD} =-10V, I_s=0A, *f*=1MHz
C_{dgo}	Source to Gate Capacitance			8	pF	V_{GS} =-10V, I_D=0A, *f*=1MHz

Typical Characteristics

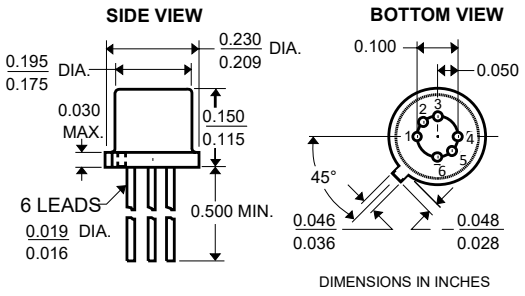
Output Characteristics
VCR11N



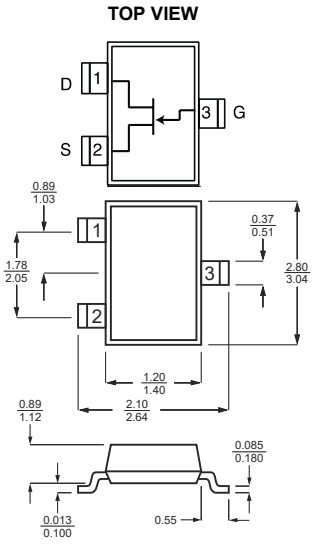


Standard Package Dimensions

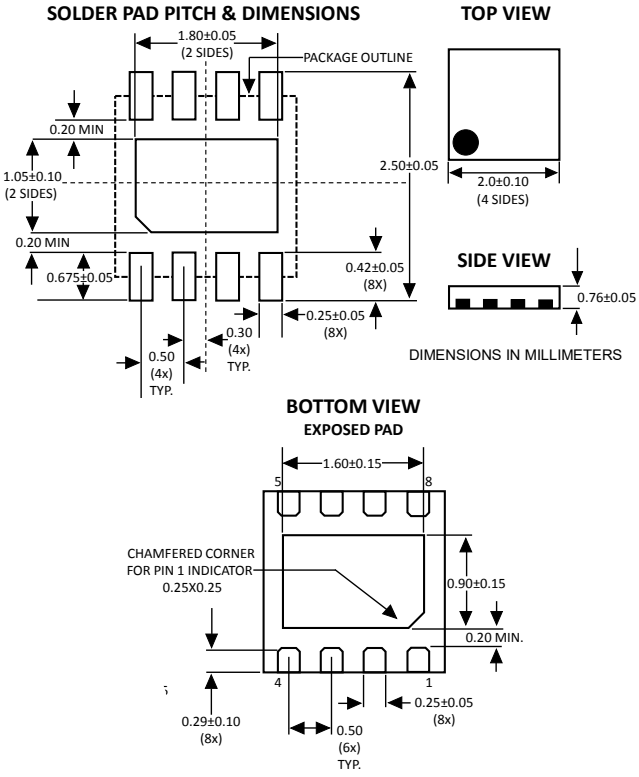
TO-71 6 Lead



SOT-23 6 Lead



DFN 8 Lead



Ordering Information

STANDARD PART CALL-OUT
VCR11N TO-71 6L RoHS
VCR11N SOT-23 6L RoHS
VCR11N DFN 8L RoHS
CUSTOM PART CALL-OUT
(CUSTOM PARTS INCLUDE SEL + 4 DIGIT NUMERIC CODE)
VCR11N TO-71 6L RoHS SELXXXX
VCR11N SOT-23 6L RoHS SELXXXX
VCR11N DFN 8L RoHS SELXXXX

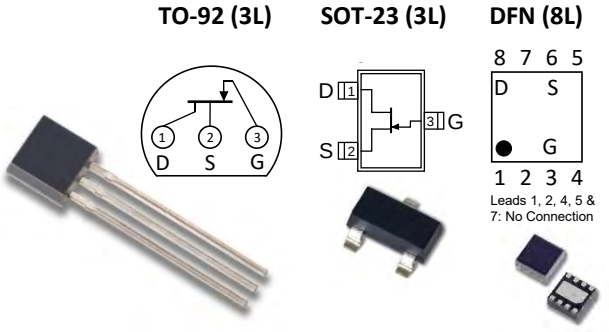
Notes

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300μs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.
4. When ordering include the full Linear Systems part number and package type. Linear Systems creates custom parts on a case by case basis. To learn whether Linear Systems can meet your requirements, please send your drawing along with a detailed description of the device specifications to sales@linearsystems.com. One of our qualified representatives will contact you.
5. All standard parts are RoHS compliant. Contact the factory for availability of non-RoHS parts.
6. Information furnished by Linear Integrated Systems is believed to be accurate and reliable. However, no responsibility is assumed for its use; nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Linear Integrated Systems.

LS26VNS

N-Channel JFET, Voltage Controlled Resistor

ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +135°C
Maximum Power Dissipation	
Continuous Power Dissipation @ Ta= +25°C	350mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = -40V
Gate to Drain	V_{GDS} = -40V



Features

- Continuous Voltage-Controlled Resistance
- High Off-Isolation
- High Input Impedance
- Gain Ranging Capability
- Simplified Drive Voltage Capabilities
- No Circuit Interaction
- Wide Range Signal Attenuation

Benefits

- Wide Range Signal Attenuation
- Gain Ranging
- Simplified Gate Drive
- High Breakdown Voltage
- No Circuit Interaction

Applications

- Variable Gain Amplifiers
- Automatic Gain Control
- Voltage Controlled Oscillator
- Small Signal Attenuations
- Filter Range Control

Description

The LS26VNS N-Channel Single JFET voltage controlled resistor has a drain-source resistance that is controlled by a DC bias voltage (V_{GS}) applied to a high impedance gate terminal. Minimum RDS of 14 Ω occurs when V_{GS} = -1.0V. As V_{GS} approaches the pinch-off voltage of -6.0V RDS rapidly increases to the maximum value or RDS = 38 Ω.

The LS26VNS is specially intended for applications where the drain-source voltage is a low-level AC signal with no DC component. The key device performance is the predictable RDS change from14 to 38 Ω with no change in V_{GS} voltage. The LS26VNS is available in TO-92 (3 Lead), SOT-23 (3 Lead) and small foot-print DFN (8 Lead) packages.

Static Electrical Characteristics @ Tj= 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-40			V	I_G = -1µA, V_{DS} = 0V
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-1.0		-6.0	V	V_{DS} = 10V, I_D = 1µA
I_{GSS}	Gate to Source Leakage Current			-1.0	nA	V_{GS} = -20V, V_{DS} = 0V
$V_{GS(F)}$	Gate to Source Forward Voltage		0.7		V	I_G = 1mA, I_D = 0A
$R_{DS(on)1}$	Drain to Source "ON" Resistance	14		38	Ohms	V_{DS} =0.5V, I_D=2.5mA
$R_{DS(on)2}$	Drain to Source "ON" Resistance	14		38	Ohms	V_{DS} =0.5V, I_D=5.0mA
R_{DS1}/R_{DS2}	Static $R_{DS(on)}$ Ratio	0.90		1.0		

Dynamic Electrical Characteristics @ 25°C (unless otherwise stated)

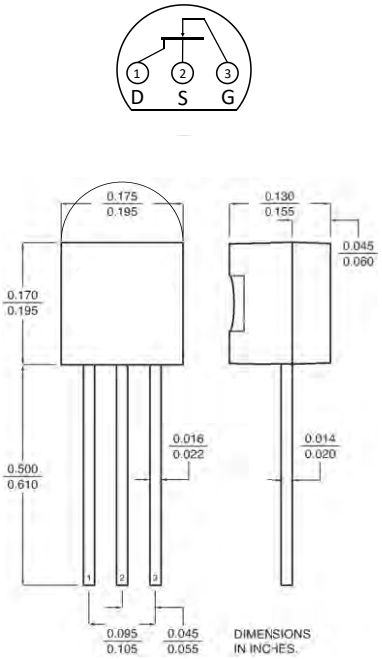
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$R_{DS(on)ac}$	Drain to Source "ON" Resistance	14		38	Ohms	V_{DS} = 0.50V, I_D = 300 µA, *f* = 1kHz
C_{ISS}	Common Source Input Capacitance		13		pF	V_{DS} = 20V, V_{GS} = 0V, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Cap.		3.6		pF	V_{DS} = 0V, V_{GS} = -12V , *f* = 1MHz

Notes

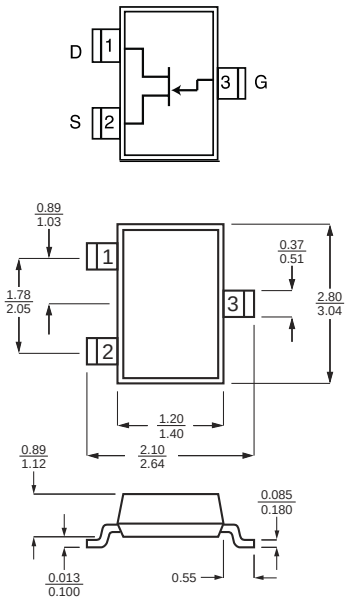
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

Package Dimensions

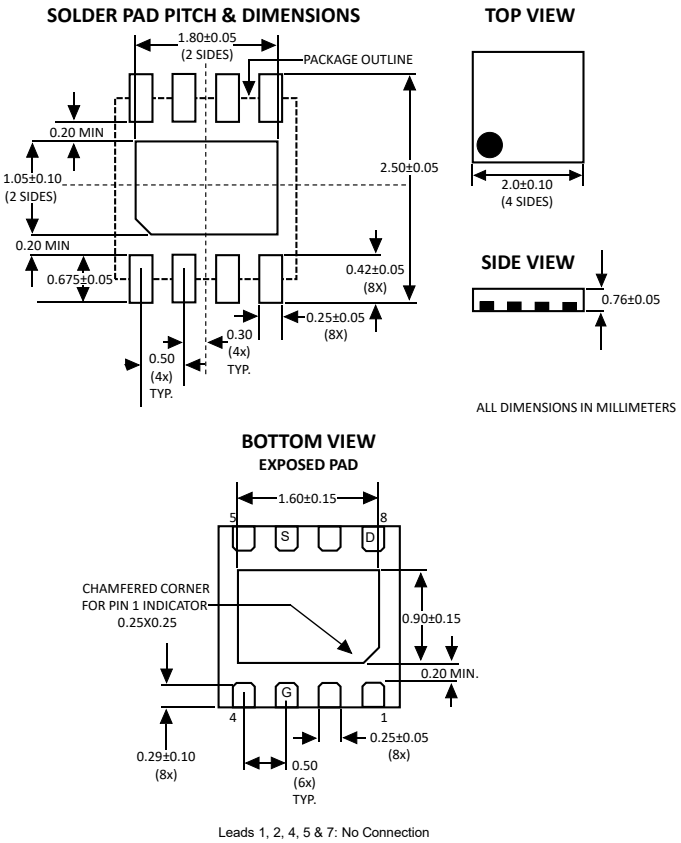
TO-92 3 Lead



SOT-23 3 Lead

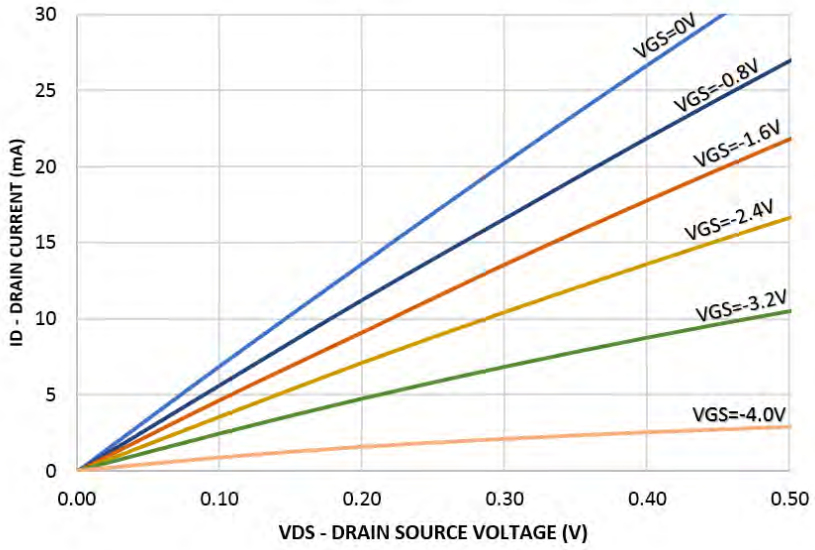


DFN 8 Lead



Typical Characteristics

Output Characteristics
LS26VNS



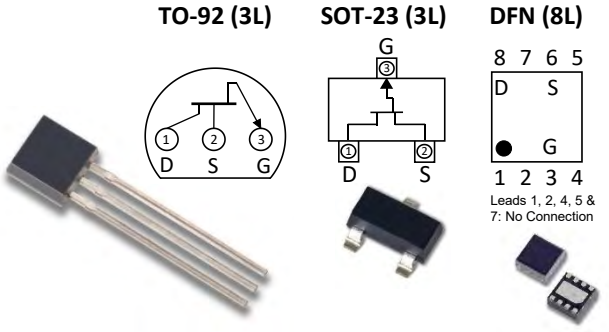
Ordering Information

STANDARD PART CALL-OUT
LS26VNS TO-92 3L RoHS
LS26VNS SOT-23 3L RoHS
LS26VNS DFN 8L RoHS
CUSTOM PART CALL-OUT
(CUSTOM PARTS INCLUDE SEL + 4 DIGIT NUMERIC CODE)
LS26VNS TO-92 3L RoHS SELXXXX
LS26VNS SOT-23 3L RoHS SELXXXX
LS26VNS DFN 8L RoHS SELXXXX

LS26VPS

P-Channel JFET, Voltage Controlled Resistor

ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +135°C
Maximum Power Dissipation	
Continuous Power Dissipation @ Ta= +25°C	350mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = +40V
Gate to Drain	V_{GDS} = +40V



Features

- Continuous Voltage-Controlled Resistance
- High Off-Isolation
- High Input Impedance
- Gain Ranging Capability
- Simplified Drive Voltage Capabilities
- No Circuit Interaction
- Wide Range Signal Attenuation

Benefits

- Wide Range Signal Attenuation
- Gain Ranging
- Simplified Gate Drive
- High Breakdown Voltage
- No Circuit Interaction

Applications

- Variable Gain Amplifiers
- Automatic Gain Control
- Voltage Controlled Oscillator
- Small Signal Attenuations
- Filter Range Control

Description

The LS26VPS P-Channel Single JFET voltage-controlled resistor has a drain-source resistance that is controlled by a DC bias voltage (V_{GS}) applied to a high impedance gate terminal. Minimum RDS of 20 Ω occurs when V_{GS} = 3.0V. As V_{GS} approaches the pinch-off voltage of 7.5V, RDS rapidly increases to the maximum value or RDS = 50 Ω.

The LS26VPS is specially intended for applications where the drain-source voltage is a low-level AC signal with no DC component. The key device performance is the predictable RDS change from 20 to 50 Ω with no change in V_{GS} voltage. The LS26VPS is available in TO-92 (3 Lead), SOT-23 (3 Lead) and small foot-print DFN (8 Lead) packages.

Static Electrical Characteristics @ Tj= 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	+40			V	I_G = +1μA, V_{DS} = 0V
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	3.0		7.5	V	V_{DS} = -10V, I_D = -1μA
I_{GSS}	Gate to Source Leakage Current			1.0	nA	V_{GS} = +20V, V_{DS} = 0V
$V_{GS(F)}$	Gate to Source Forward Voltage		0.7		V	I_G = 1mA, I_D = 0A
$R_{DS(on)1}$	Drain to Source "ON" Resistance	20	35	50	Ohms	V_{DS} = -0.5V, I_D= -2.5mA
$R_{DS(on)2}$	Drain to Source "ON" Resistance	20		50	Ohms	V_{DS} = -0.5V, I_D= -5.0mA
R_{DS1}/R_{DS2}	Static $R_{DS(on)}$ Ratio	0.90		1.0		

Dynamic Electrical Characteristics @ 25°C (unless otherwise stated)

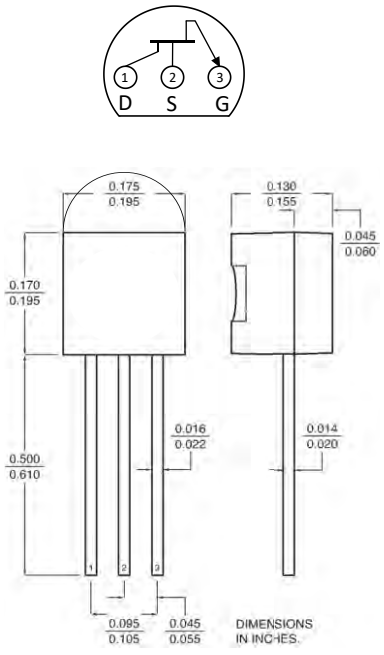
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$R_{DS(on)ac}$	Drain to Source "ON" Resistance	20		50	Ohms	V_{DS} = -0.50V, I_D = -300 µA, *f* = 1kHz
C_{ISS}	Common Source Input Capacitance		13		pF	V_{DS} = -20V, V_{GS} = 0V, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Cap.		3.6		pF	V_{DS} = 0V, V_{DS} = +12V , *f* = 1MHz

Notes

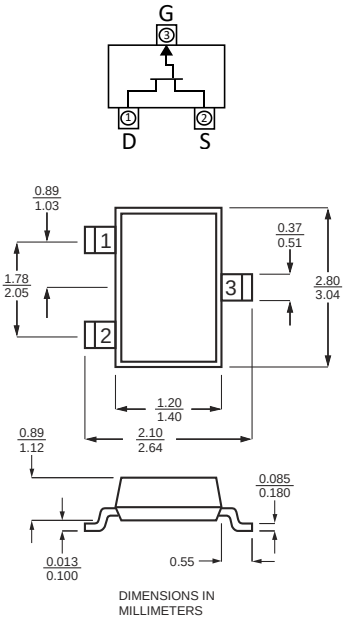
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

Package Dimensions

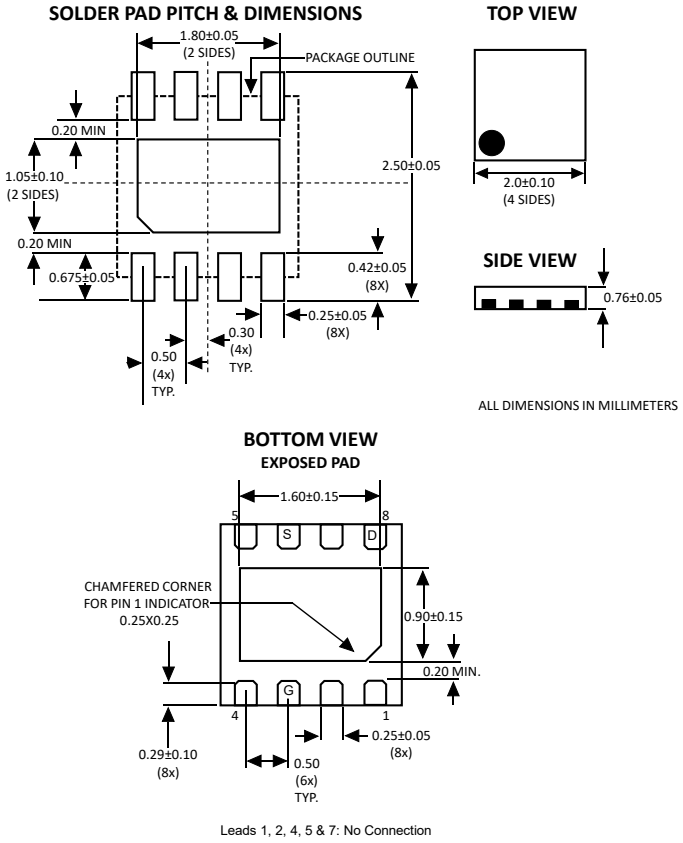
TO-92 3 Lead



SOT-23 3 Lead

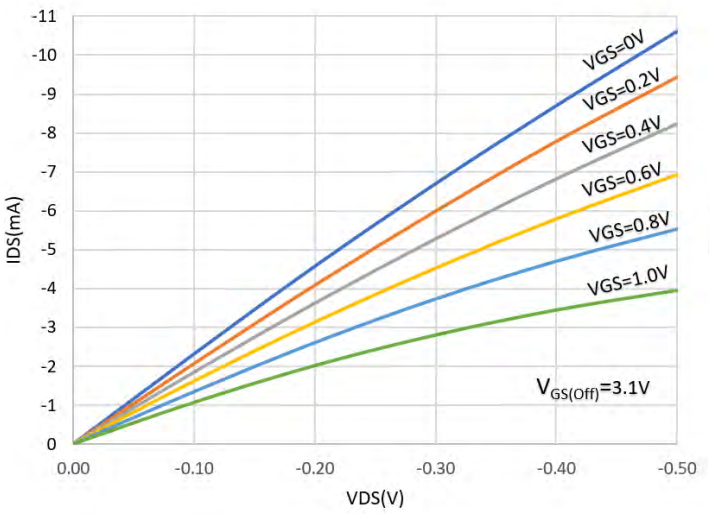


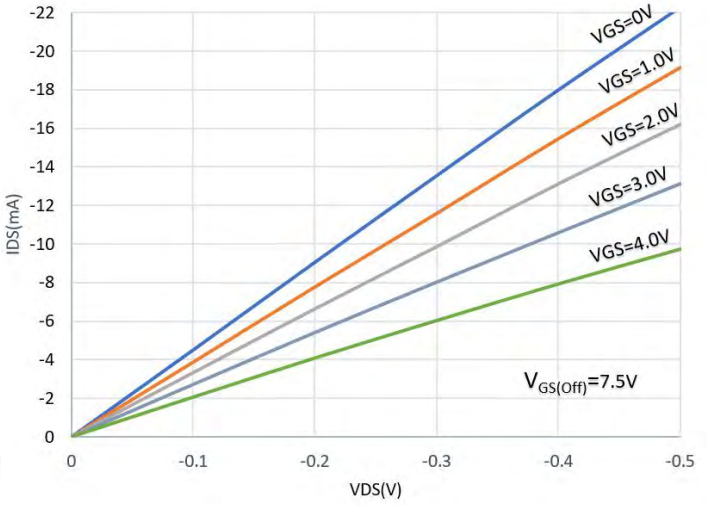
DFN 8 Lead



Typical Characteristics

Output Characteristics
LS26VPS



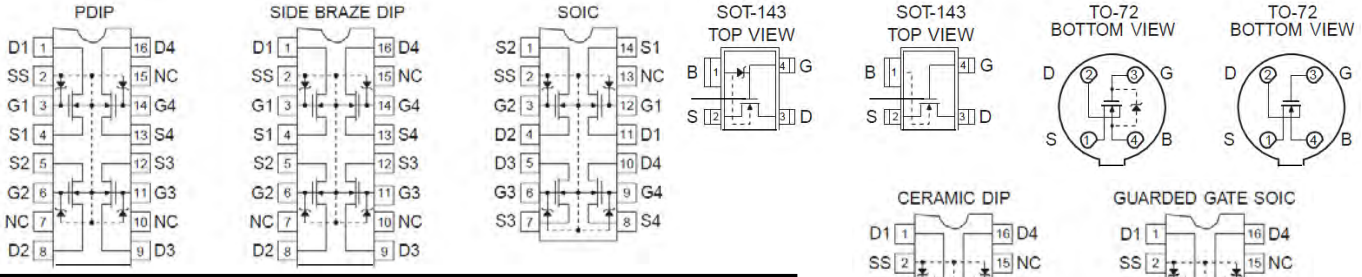


Ordering Information

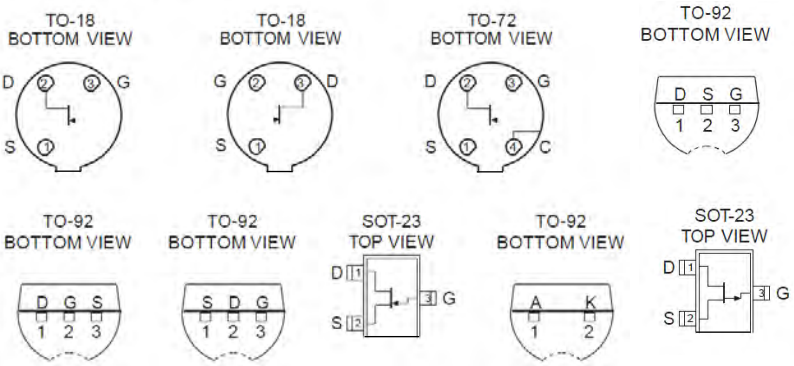
STANDARD PART CALL-OUT
LS26VPS TO-92 3L RoHS
LS26VPS SOT-23 3L RoHS
LS26VPS DFN 8L RoHS
CUSTOM PART CALL-OUT
(CUSTOM PARTS INCLUDE SEL + 4 DIGIT NUMERIC CODE)
LS26VPS TO-92 3L RoHS SELXXXX
LS26VPS SOT-23 3L RoHS SELXXXX
LS26VPS DFN 8L RoHS SELXXXX

Package Options

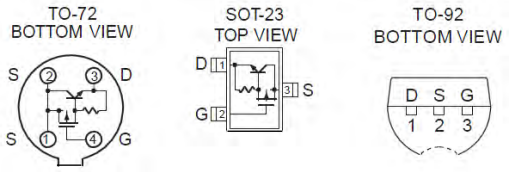
Lateral DMOS Switch Packages



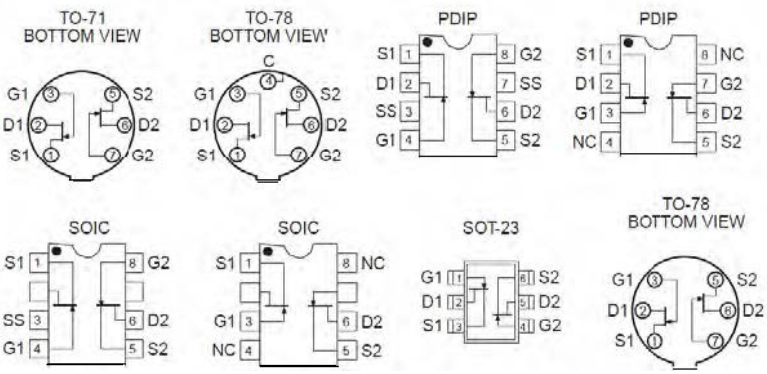
Single JFET Packages



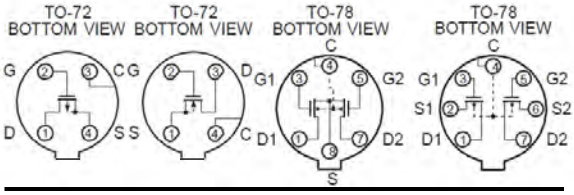
BIFET Amplifier Packages



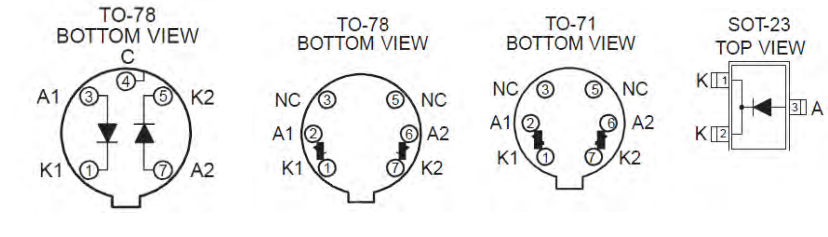
Dual JFET Packages

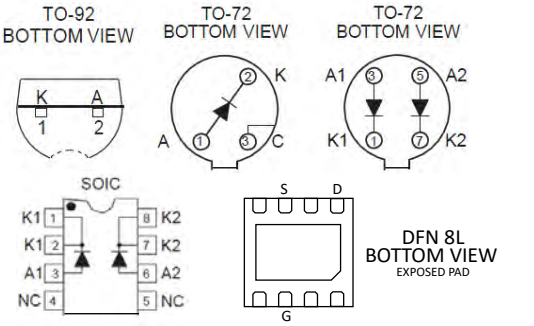


MOSFET Packages



Diode Packages





BJT Packages